R8822

16-Bit RISC Microcontroller User's Manual

RDC ***RISC DSP Controller***

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Contents

1. Features 5

2. Block Diagram 6

3. Pin Configuration 7

3.1 PQFP 7
3.2 LQFP 8
3.3 R8822 PQFP & LQFP Pin Out Table 9

4. Pin Description 10

4.1 R8822 I/O Characteristics of Each Pin 16

5. Basic Application System Block 19

6. Read/Write Timing Diagram 21

7. Crystal Characteristics 23

8. Execution Unit 24

8.1 General Registers 24
8.2 Segment Registers 25
8.3 Instruction Pointer and Status Flags Registers 25
8.4 Address Generation 27

9. Peripheral Control Block Registers 28

10. Power Save & Power Down 30

11. Reset 33

12. Bus Interface Unit 35

12.1 Memory and I/O Interface 35

12.2 Data Bus....36
12.3 Wait States....36
12.4 Bus Hold....36
12.5 Bus Width....38

13. Chip Select Unit....40

13.1 $\overline{\text{UCS}}$....40

13.2 $\overline{\text{LCS}}$....41

13.3 $\overline{\text{MCSx}}$....42

13.4 $\overline{\text{PCSx}}$....44

14. Interrupt Controller Unit....46

14.1 Master Mode and Slave Mode....46
14.2 Interrupt Vector, Type and Priority....48
14.3 Interrupt Requests....48
14.4 Interrupt Acknowledge....48
14.5 Programming the Registers....49

15. DMA Unit....63

15.1 DMA Operation....63
15.2 External Requests....68
15.3 Serial Port/DMA Transfer....70

16. Timer Control Unit....71

16.1 Timer/Counter Unit Output Mode....75

17. Watchdog Timer....76

18. Asynchronous Serial Ports....78

18.1 Serial Port Flow Control....78
18.1.1 DCE/DTE Protocol....79
18.1.2 CTS/RTR Protocol....79
18.2 DMA Transfer to/from a Serial Port Function....80

18.3 The Asynchronous Mode Description 80

19. PIO Unit 85

19.1 PIO Multi-Function Pin List Table 85

20. DRAM Controller 89

20.1 Programmable Read/ Write Cycle Time 89
20.2 Programmable Refresh Control 90

21. Instruction Set OPCodes and Clock Cycles 91

22. R8822 Execution Timings 95

23. DC Characteristics 96

23.1 Absolute Maximum Rating 96
23.2 Recommended DC Operating Conditions 96
23.3 DC Electrical Characteristics 96

24. AC Characteristics 97

25. Thermal Characteristics 111

26. Package Information 112

26.1 PQFP 112
26.2 LQFP 113

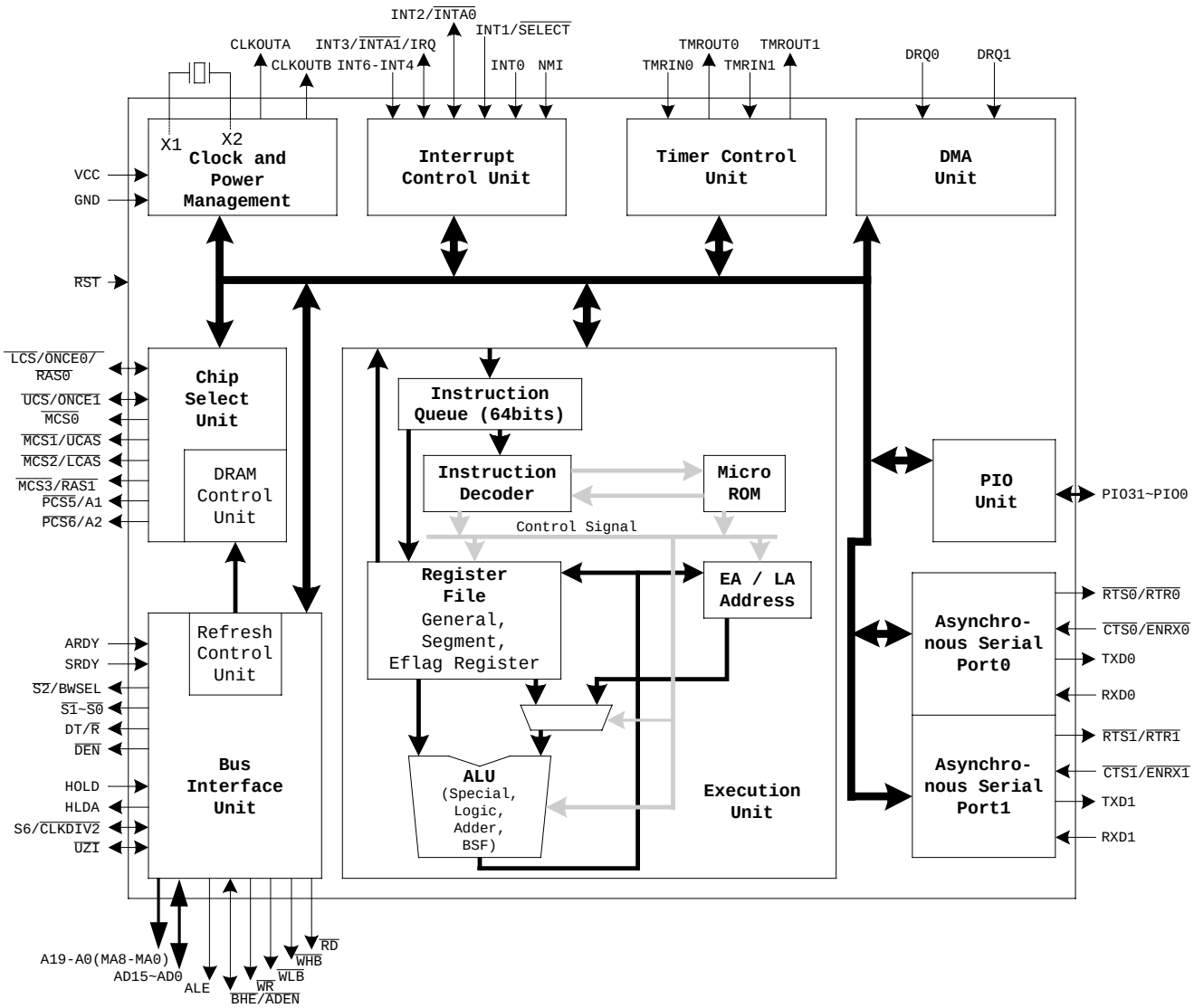
27. Revision History 114

16-Bit Microcontroller with 8-bit or 16-bit dynamic external data bus

1. Features

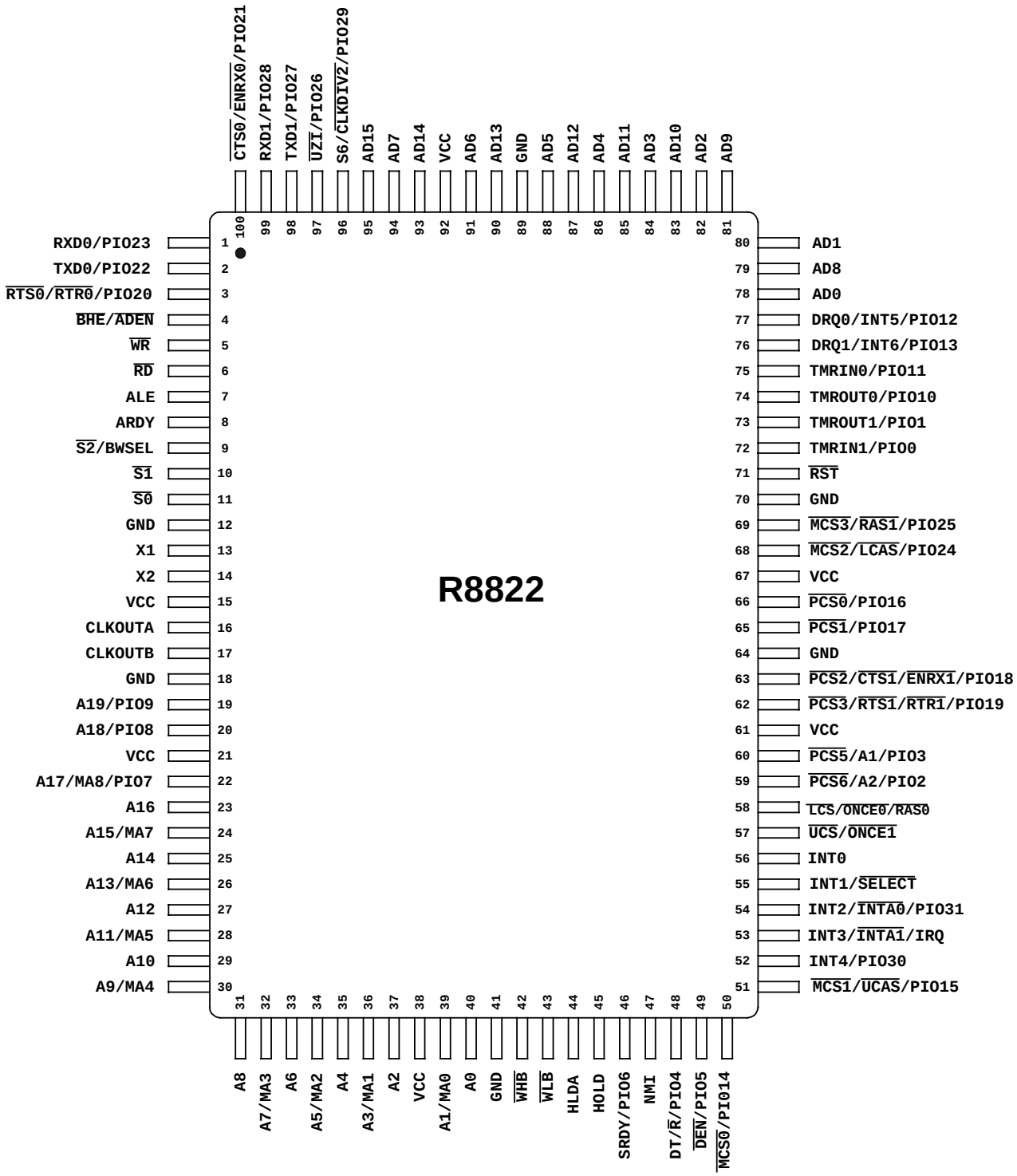
- Five-stage pipeline
- RISC architecture
- Static Design & Synthesizable design
- Bus interface
  - Multiplexed address and Data bus
  - Supports non-multiplexed address bus A [19:0]
  - 8-bit or 16-bit external bus dynamic access
  - 1M-byte memory address space
  - 64K-byte I/O space
- Software is compatible with the 80C186 microprocessor
- Supports two Asynchronous serial channels with hardware handshaking signals.
- Support CPU ID
- Supports 32 PIO pins
- Supports 64kx16, 128kx16, 256kx16 EDO or FP DRAM with auto-refresh control
- Three independent 16-bit timers and one independent programmable watchdog timer
- The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable wait-state generator
- With 8-bit or 16-bit Boot ROM bus size

2. Block Diagram

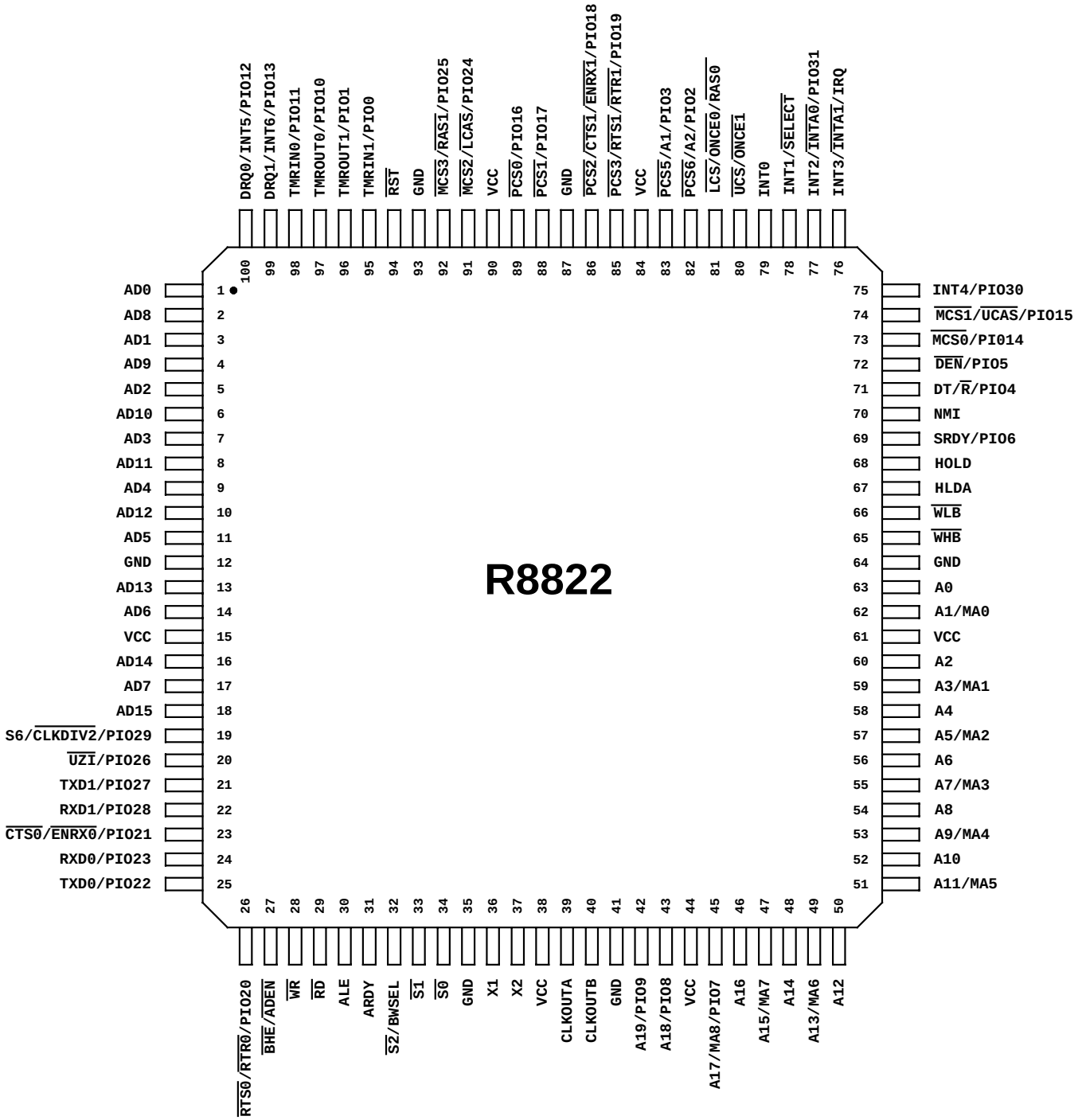


3. Pin Configuration

3.1 PQFP



3.2 LQFP


R8822
1 AD0
2 AD8
3 AD1
4 AD9
5 AD2
6 AD10
7 AD3
8 AD11
9 AD4
10 AD12
11 AD5
12 GND
13 AD13
14 AD6
15 VCC
16 AD14
17 AD7
18 AD15
19 S6/CLKDIV2/PIO29
20 UZI/PIO26
21 TXD1/PIO27
22 RXD1/PIO28
23 CTS0/ENRX0/PIO21
24 RXD0/PIO23
25 TXD0/PIO22
26 RTS0/RTR0/PIO20
27 BHE/ADEN
28 WR
29 RD
30 ALE
31 ARDY
32 S2/BWSEL
33 S1
34 S0
35 GND
36 X1
37 X2
38 VCC
39 CLKOUTA
40 CLKOUTB
41 GND
42 A19/PIO9
43 A18/PIO8
44 VCC
45 A17/MA8/PIO7
46 A16
47 A15/MA7
48 A14
49 A13/MA6
50 A12
51 A11/MA5
52 A10
53 A9/MA4
54 A8
55 A7/MA3
56 A6
57 A5/MA2
58 A4
59 A3/MA1
60 A2
61 VCC
62 A1/MA0
63 A0
64 GND
65 WHB
66 WLB
67 HLDA
68 HOLD
69 SRDY/PIO6
70 NMI
71 DT/R/PIO4
72 DEN/PIO5
73 MCS0/PI014
74 MCS1/UCAS/PIO15
75 INT4/PIO30
76 INT3/INTA1/IRQ
77 INT2/INTA0/PIO31
78 INT1/SELECT
79 INT0
80 UCS/ONCE1
81 LCS/ONCE0/RAS0
82 PCS6/A2/PIO2
83 PCS5/A1/PIO3
84 VCC
85 PCS3/RTS1/RTR1/PIO19
86 PCS2/CTS1/ENRX1/PIO18
87 GND
88 PCS1/PIO17
89 PCS0/PIO16
90 VCC
91 MCS2/LCAS/PIO24
92 MCS3/RAS1/PIO25
93 GND
94 RST
95 TMRIN1/PIO0
96 TMROUT1/PIO1
97 TMROUT0/PIO10
98 TMRIN0/PIO11
99 DRQ1/INT6/PIO13
100 DRQ0/INT5/PIO12

3.3 R8822 PQFP & LQFP Pin Out Table

Pin name	LQFP Pin No.	PQFP Pin No.	Pin name	LQFP Pin No.	PQFP Pin No.
AD0	1	78	A11/MA5	51	28
AD8	2	79	A10	52	29
AD1	3	80	A9/MA4	53	30
AD9	4	81	A8	54	31
AD2	5	82	A7/MA3	55	32
AD10	6	83	A6	56	33
AD3	7	84	A5/MA2	57	34
AD11	8	85	A4	58	35
AD4	9	86	A3/MA1	59	36
AD12	10	87	A2	60	37
AD5	11	88	VCC	61	38
GND	12	89	A1/MA0	62	39
AD13	13	90	A0	63	40
AD6	14	91	GND	64	41
VCC	15	92	$\overline{WHB}$	65	42
AD14	16	93	$\overline{WLB}$	66	43
AD7	17	94	HLDA	67	44
AD15	18	95	HOLD	68	45
S6/ $\overline{CLKDIV2}$ /PIO29	19	96	SRDY/PIO6	69	46
$\overline{UZI}$ /PIO26	20	97	NMI	70	47
TXD1/PIO27	21	98	DT/ $\overline{R}$ /PIO4	71	48
RXD1/PIO28	22	99	$\overline{DEN}$ /PIO5	72	49
$\overline{CTS0}$ / $\overline{ENRX0}$ /PIO21	23	100	$\overline{MCS0}$ /PIO14	73	50
RXD0/PIO23	24	1	$\overline{MCS1}$ / $\overline{UCAS}$ /PIO15	74	51
TXD0/PIO22	25	2	INT4/PIO30	75	52
$\overline{RTS0}$ / $\overline{RTR0}$ /PIO20	26	3	INT3/ $\overline{INTA1}$ /IRQ	76	53
$\overline{BHE}$ / $\overline{ADEN}$	27	4	INT2/ $\overline{INTA0}$ /PIO31	77	54
$\overline{WR}$	28	5	INT1/ $\overline{SELECT}$	78	55
$\overline{RD}$	29	6	INT0	79	56
ALE	30	7	$\overline{UCS}$ / $\overline{ONCE1}$	80	57
ARDY	31	8	$\overline{LCS}$ / $\overline{ONCE0}$ / $\overline{RAS0}$	81	58
$\overline{S2}$ /BWSEL	32	9	$\overline{PCS6}$ /A2/PIO2	82	59
$\overline{S1}$	33	10	$\overline{PCS5}$ /A1/PIO3	83	60
$\overline{S0}$	34	11	VCC	84	31
GND	35	12	$\overline{PCS3}$ / $\overline{RTS1}$ / $\overline{RTR1}$ PIO19	85	62
X1	36	13	$\overline{PCS2}$ / $\overline{CTS1}$ / $\overline{ENRX1}$ /PIO18	86	63
X2	37	14	GND	87	64
VCC	38	15	$\overline{PCS1}$ /PIO17	88	65
CLKOUTA	39	16	$\overline{PCS0}$ /PIO16	89	66
CLKOUTB	40	17	VCC	90	67
GND	41	18	$\overline{MCS2}$ / $\overline{LCAS}$ /PIO24	91	68
A19/PIO9	42	19	$\overline{MCS3}$ / $\overline{RAS1}$ /PIO25	92	69
A18/PIO8	43	20	GND	93	70
VCC	44	21	$\overline{RST}$	94	71
A17/MA8/PIO7	45	22	TMRI N1/PI O0	95	72
A16	46	23	TMROUT1/PI O1	96	73
A15/MA7	47	24	TMROUT0/PI O10	97	74
A14	48	25	TMRI N0/PI O11	98	75
A13/MA6	49	26	DRQ1/INT6/PI O13	99	76
A12	50	27	DRQ0/INT5/PI O12	100	77

4. Pin Description

Pin No. (PQFP)	Symbol	Type	Description
15, 21, 38, 61, 67, 92	VCC	Input	System power: +5 volt power supply.
12, 18, 41, 64, 70, 89	GND	Input	System ground.
71	$\overline{RST}$	Input	Reset input. When $\overline{RST}$ is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and transfers the address to the reset address FFFF0h.
13	X1	Input	Input to the oscillator amplifier.
14	X2	Output	Output from the inverting oscillator amplifier.
16	CLKOUTA	Output	Clock output A. The CLKOUTA operation is the same as crystal input frequency (X1). CLKOUTA remains active during reset and bus hold conditions.
17	CLKOUTB	Output	Clock output B. The CLKOUTB operation is the same as crystal input frequency (X1). CLKOUTB remains active during reset and bus hold conditions.
Asynchronous Serial Port Interface			
1	RXD0/PIO23	Input/Output	Receive data for asynchronous serial port 0. This pin receives asynchronous serial data.
2	TXD0/PIO22	Output/Input	Transmit data for asynchronous serial port 0. This pin transmits asynchronous serial data from the UART of the micro-controllers.
3	$\overline{RTS0}$ / $\overline{RTR0}$ /PIO20	Output/Input	Ready to send/Ready to Receive signal for asynchronous serial port 0. When the RTS0 bit in the AUXCON register is set and the FC bit in the serial port 0 control register is set, the $\overline{RTS0}$ signal is enabled. Otherwise, when the RTS0 bit is cleared and the FC bit is set, the $\overline{RTR0}$ signal is enabled.
100	$\overline{CTS0}$ / $\overline{ENRX0}$ /PIO21	Input/Output	Clear to send/Enable Receiver Request signal for asynchronous serial port 0. When the ENRX0 bit in the AUXCON register is cleared and the FC bit in the serial port 0 control register is set, the $\overline{CTS0}$ signal is enabled. Otherwise, when the ENRX0 bit is set and the FC bit is set, the $\overline{ENRX0}$ signal is enabled.
98	TXD1/PIO27	Output/Input	Transmit data for asynchronous serial port 1. This pin transmits asynchronous serial data from the UART of the micro-controllers.
99	RXD1/PIO28	Input/Output	Receive data for asynchronous serial port 1. This pin receives asynchronous serial data.
62	$\overline{PCS3}$ / $\overline{RTS1}$ / $\overline{RTR1}$ /PIO18	Output/Input	Ready to send/Ready to Receive signal for asynchronous serial port 1. When the RTS1 bit in the AUXCON register is set and the FC bit in the serial port 1 control register is set, the $\overline{RTS1}$ signal is enabled. Otherwise, when the RTS1 bit is cleared and the FC bit is set, the $\overline{RTR1}$ signal is enabled.

<table>
<tr><td>63</td><td>$\overline{PCS2}$ / $\overline{CTS1}$ / $\overline{ENRX1}$ /PIO19</td><td>Input/Output</td><td>Clear to send/Enable Receiver Request signal for asynchronous serial port 1. When the ENRX1 bit in the AUXCON register is cleared and the FC bit in the serial port 1 control register is set, the $\overline{CTS1}$ signal is enabled. Otherwise, when the ENRX1 bit is set and the FC bit is set, the $\overline{ENRX1}$ signal is enabled.</td></tr>
<tr><td colspan="4">Bus Interface</td></tr>
<tr><td>4</td><td>$\overline{BHE}$ / $\overline{ADEN}$</td><td>Output/Input</td><td>Bus high enable/address enable. During a memory access, the $\overline{BHE}$ and (AD0 or A0) encodings indicate what types of the bus cycle. $\overline{BHE}$ is asserted during T1 and keeps the asserted to T3 and Tw. This pin is floating during a bus hold and reset.
<table>
<tr><td colspan="3">$\overline{BHE}$ and (AD0 or A0) Encodings</td></tr>
<tr><td>$\overline{BHE}$</td><td>AD0 or A0</td><td>Types of Bus Cycle</td></tr>
<tr><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>1</td><td>High byte transfer (D15-D8)</td></tr>
<tr><td>1</td><td>0</td><td>Low byte transfer (D7-D0)</td></tr>
<tr><td>1</td><td>1</td><td>Refresh</td></tr>
</table>
The address portion of the AD bus can be enabled or disabled by DA bit in the LMCS and UMCS register during LCS or UCS bus cycle access if $\overline{BHE}$ / $\overline{ADEN}$ is held high during power-on reset. No external pull-up resistor is required because the $\overline{BHE}$ / $\overline{ADEN}$ has an internal weak pull-up resistor. The AD bus always drives both address and data during LCS or UCS bus cycle access if the $\overline{BHE}$ / $\overline{ADEN}$ pin is with an external pull-low resistor during reset.</td></tr>
<tr><td>5</td><td>$\overline{WR}$</td><td>Output</td><td>Write Strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active during T2, T3 and Tw of any write cycle, and floats during a bus hold or reset.</td></tr>
<tr><td>6</td><td>$\overline{RD}$</td><td>Output</td><td>Read Strobe. It's an active low signal which indicates that the micro-controller is performing a memory or I/O read cycle. $\overline{RD}$ floats during a bus hold or reset.</td></tr>
<tr><td>7</td><td>ALE</td><td>Output</td><td>Address latch enable. Active high. This pin indicates that an address output on the AD bus. Address is guaranteed to be valid on the trailing edge of ALE. This pin is tri-stated during ONCE mode and is never floating during a bus hold or reset.</td></tr>
<tr><td>8</td><td>ARDY</td><td>Input</td><td>Asynchronous ready. This pin performs the microcontroller that the address memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active high. The falling edge of ARDY must be synchronized to CLKOUTA. Tie ARDY high, so the microcontroller is always asserted in the ready condition. If the ARDY is not used, tie this pin low to yield control to SRDY.
Both SRDY and ARDY should be tied to high if the system need not assert wait states by externality.</td></tr>
</table>

<table>
<tr><td>9
10
11</td><td>$\overline{S2}$ /BWSEL
$\overline{S1}$
$\overline{S0}$</td><td>Output/Input
Output
Output</td><td>Bus cycle status. These pins are encoded to indicate the bus status. $\overline{S2}$ can be used as memory or I/O indicator. $\overline{S1}$ can be used as DT/$\overline{R}$ indicator. These pins are floating during a bus hold and reset.
The $\overline{S2}$ /BWSEL is to decide the boot ROM bus width when $\overline{RST}$ pin goes from low to high. If $\overline{S2}$ /BWSEL is with a pull-low resistor (330 ohm), the boot ROM bus width is 8 bits. Otherwise, the boot ROM bus width is 16 bits.
Bus Cycle Encoding Description
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read data from I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write data to I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read data from memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write data to memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
</td></tr>
<tr><td>19
20
22
23
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25
26
27
28
29
30
31
32
33
34
35
36
37
39
40</td><td>A19/PIO9
A18/PIO8
A17/MA8/PIO7
A16
A15/MA7
A14
A13/MA6
A12
A11/MA5
A10
A9/MA4
A8
A7/MA3
A6
A5/MA2
A4
A3/MA1
A2
A1/MA0
A0</td><td>Output/Input</td><td>Address bus. Non-multiplexed memory or I/O addresses. The A bus is one-half of a CLKOUTA period earlier than the AD bus. These pins are in high-impedance states during a bus hold or reset.

MA8-MA0: DRAM address interface. The MA bus is multiplexed with A bus. When accessing DRAM, the bus performs row or column address, otherwise the bus performs Address bus.</td></tr>
<tr><td>78,80,82,84,86,88
91,94
79,81,83,85,87,90
93,95</td><td>AD0-AD7

AD8-AD15</td><td>Input/Output</td><td>The multiplexed address and data bus for memory or I/O accessing. The address is present during the t1 clock phase, and the data bus phase is in t2-t4 cycle.
The address phase of the AD bus can be disabled when the $\overline{BHE}$ / $\overline{ADEN}$ pin is with an external pull-low resistor during reset.
The AD bus is in high-impedance state during a bus hold or reset conditions and this bus is also used to load system configuration information (with pull-up or pull-low resistors) into the RESCON register when the reset input goes from low to high.</td></tr>
<tr><td>42</td><td>$\overline{WHB}$</td><td>Output</td><td>Write high byte. This pin indicates the high byte data (AD15-AD8) on the bus is to be written to a memory or I/O device.
$\overline{WHB}$ is the logic OR of $\overline{BHE}$ and $\overline{WR}$.
This pin is floating during reset or bus hold conditions.</td></tr>
</table>

43	$\overline{WLB}$	Output	Write low byte. This pin indicates the low byte data (AD7-AD0) on the bus is to be written to a memory or I/O device. $\overline{WLB}$ is the logic OR of $\overline{WR}$ and A0. This pin is floating during reset or bus holds.
44	HLDA	Output	Bus hold acknowledge. Active high. The microcontroller will issue an HLDA in response to a HOLD request by external bus master at the end of T4 or Ti. When the microcontroller is in hold status (HLDA is high), AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{S0}$ - $\overline{S1}$, S6, $\overline{BHE}$, DT/$\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}$ - $\overline{PCS5}$, $\overline{MCS3}$ - $\overline{MCS0}$ and $\overline{PCS3}$ - $\overline{PCS0}$ will be driven high. After HOLD is detected as being low, the microcontroller will lower HLDA.
45	HOLD	Input	Bus Hold request. Active high. This pin indicates that another bus master is requesting the local bus.
46	SRDY/PIO6	Input/Output	Synchronous ready. This pin performs the microcontroller that the address memory space or I/O device will complete a data transfer. The SRDY pin accepts a falling edge that is asynchronous to CLKOUTA and is active high. SRDY is accomplished by elimination of the one-half clock period required to internally synchronize ARDY. Tie SRDY high, so the microcontroller is always asserted in the ready condition. If the SRDY is not used, tie this pin low to yield control to ARDY. Both SRDY and ARDY should be tied to high if the system need not assert wait states by externality.
48	DT/$\overline{R}$/PIO4	Output/Input	Data transmit or receive. This pin indicates the direction of data flow through an external data-bus transceiver. When DT/$\overline{R}$ is asserted low, the microcontroller receives data. When DT/R is asserted high, the microcontroller writes data to the data bus.
49	$\overline{DEN}$/PIO5	Output/Input	Data enable. This pin is provided as a data bus transceiver output enable. $\overline{DEN}$ is asserted during memory and I/O accesses. $\overline{DEN}$ is driven high when DT/$\overline{R}$ changes states. It is floating during bus hold or reset conditions.
96	S6/$\overline{CLKDIV2}$/PIO29	Output/Input	Bus cycle status bit6/clock divided by 2. For the S6 feature, this pin is set to low to indicate a microcontroller-initiated bus cycle or high to indicate a DMA-initiated bus cycle during T2, T3, Tw and T4. For $\overline{CLKDIV2}$ feature. The internal clock of microcontroller is the external clock divided by 2. (CLKOUTA, CLKOUTB=X1/2), if this pin held low during power-on reset. The pin is sampled on the rising edge of $\overline{RST}$.
97	$\overline{UZI}$/PIO26	Output/Input	Upper zero indication. This pin is the logical OR of the inverted A19-A16. It is asserted in the T1 and is held throughout the cycle.
Chip Select Unit Interface			
50 51 68 69	$\overline{MCS0}$/PIO14 $\overline{MCS1}$ / $\overline{UCAS}$/PIO15 $\overline{MCS2}$ / $\overline{LCAS}$/PIO24 $\overline{MCS3}$ / $\overline{RAS1}$/PIO25	Output/Input	Midrange memory chip selects. For $\overline{MCS}$ feature, these pins are active low when the MMCS register is enabled to access a memory. The address ranges are programmable. $\overline{MCS3}$ - $\overline{MCS0}$ are held high during bus holds.

			When the bit6 of UMCS (A0h) register is set to 1, the $\overline{UCS}$ will be disabled and the $\overline{MCS3}$ - $\overline{MCS1}$ will be activated as bank1 control signals $\overline{RAS1}$, $\overline{LCAS}$ and $\overline{UCAS}$ of DRAM controller. The DRAM memory is located from 80000h to FFFFFh.
57	$\overline{UCS}$ / $\overline{ONCE1}$	Output/Input	Upper memory chip select/ONCE mode request 1. For $\overline{UCS}$ feature, this pin acts low when the system accesses the defined portion memory block of the upper 512K bytes (80000h-FFFFFh) memory region. $\overline{UCS}$. default active address region is from F0000h to FFFFFh after power-on reset. The address range for $\overline{UCS}$ is programmed by software. For $\overline{ONCE1}$ feature. If $\overline{ONCE0}$ and $\overline{ONCE1}$ are sampled low on the rising edge of $\overline{RST}$. The microcontroller enters ONCE mode. In ONCE mode, all pins are high-impedance. This pin incorporates a weakly pulled-up resistor.
58	$\overline{LCS}$ / $\overline{ONCE0}$ / $\overline{RAS0}$	Output/Input	Lower memory chip select/ONCE mode request 0. For $\overline{LCS}$ feature, this pin acts low when the microcontroller accesses the defined portion memory block of the lower 512K (00000h-7FFFFh) memory region. The address range for $\overline{LCS}$ is programmed by software. For $\overline{ONCE0}$ feature, see $\overline{UCS}$ / $\overline{ONCE1}$ description. This pin incorporates a weakly pulled-up resistor. When the bit 6 of LMCS (A2h) register is set to 1, this pin will act as $\overline{RAS0}$ which is the raw address of DRAM bank 0.
59 60	$\overline{PCS6}$ /A2/PIO2 $\overline{PCS5}$ /A1/PIO3	Output/Input	Peripheral chip selects/latched address bit. For $\overline{PCS}$ feature, these pins act low when the microcontroller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of $\overline{PCS}$ is programmable. These pins are asserted with the AD address bus and are not floating during bus holds. For latched address bit feature. These pins output the latched address A2 and A1 when the EX bit in the $\overline{PCS}$ and $\overline{MCS}$ auxiliary register is cleared. The A2 and A1 retain previous latched data during bus holds.
62 63 65 66	$\overline{PCS3}$ / $\overline{RTS1}$ / $\overline{RTR1}$ /PIO19 $\overline{PCS2}$ / $\overline{CTS1}$ / $\overline{ENRX1}$ /PIO18 $\overline{PCS1}$ /PIO17 $\overline{PCS0}$ /PIO16	Output/Input	Peripheral chip selects. These pins act low when the microcontroller accesses the defined memory area of the peripheral memory block (I/O or memory address). For I/O accessed, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address accesses, the base address can be located in the 1M-byte memory address region. These pins are asserted with the multiplexed AD address bus and are not floating during bus holds.
Interrupt Control Unit Interface			
47	NMI	Input	Non-maskable Interrupt. The NMI is the highest priority hardware interrupt and is non-maskable. When this pin is asserted (NMI transition from low to high), the microcontroller always transfers the address bus to the location specified by the non-maskable interrupt vector in the microcontroller interrupt vector table. The NMI pin must be

			asserted for at least one CLKOUTA period to guarantee that the interrupt is recognized.
52	INT4/PIO30	Input/Output	Maskable interrupt request 4. Active high. This pin indicates that an interrupt request has occurred. The microcontroller will jump to the INT4 address vector to execute the service routine if the INT4 is enabled. The interrupt input can be configured to be either edge- or level-triggered. The requesting device must hold INT4 until the request is acknowledged to guarantee interrupt recognition.
53	INT3/ $\overline{\text{INTA1}}$ /IRQ	Input/Output	Maskable interrupt request 3/interrupt acknowledge 1/slave interrupt request. For INT3 feature, except the differences in the interrupt line and interrupt address vector, the function of INT3 is the same as that of INT4. For $\overline{\text{INTA1}}$ feature, in cascade mode or special fully-nested mode, this pin corresponds to INT1. For IRQ feature, when the microcontroller is as a slave device, this pin issues an interrupt request to the master interrupt controller.
54	INT2/ $\overline{\text{INTA0}}$ /PIO31	Input/Output	Maskable interrupt request 2/interrupt acknowledge 0. For INT2 feature, except the differences in interrupt line and interrupt address vector, the function of INT2 is the same as that of INT4. For $\overline{\text{INTA0}}$ feature, in cascade mode or special fully-nested mode, this pin corresponds to INT0.
55	INT1/ $\overline{\text{SELECT}}$	Input/Output	Maskable interrupt request 1/slave select. For INT1 feature, except the differences in interrupt line and interrupt address vector, the function of INT1 is the same as that of INT4. For $\overline{\text{SELECT}}$ feature, when the microcontroller is as a slave device, this pin is driven from the master interrupt controller decoding. This pin is activated to indicate that an interrupt appears on the address and data bus. INT0 must be activated before $\overline{\text{SELECT}}$ is activated when the interrupt type appears on the bus.
56	INT0	Input/Output	Maskable interrupt request 0. Except the differences in interrupt line and interrupt address vector, the function of INT0 is the same as that of INT4.
Timer Control Unit Interface			
72 75	TMRIN1/PIO0 TMRIN0/PIO11	Input/Output	Timer input. These pins can be as clock or control signal input, which depend upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. These pins must be pulled-up if not being used.
73 74	TMROUT1/PIO1 TMROUT0/PIO10	Output/Input	Timer output. Depending on timer mode select, these pins provide single pulse or continuous waveforms. The duty cycle of the waveforms can be programmable. These pins float during a bus hold or reset.
DMA Unit Interface			
76 77	DRQ1/INT6/PIO13 DRQ0/INT5/PIO12	Input/Output	DMA request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals are not latched and must remain active until service finished. For INT6/INT5 function: When the DMA function is not being used, INT6/INT5 can be used as an additional external interrupt request. They share the corresponding interrupt types

			and register control bits. The INT6/5 are level-triggered only and not necessary to be held until the interrupt is acknowledged. (Such high levels keep interrupt requests.)

Notes:

1. When PIO mode and direction registers are set, 32 MUX definition pins can be set as PIO pins. For example, the DRQ1/INT6/PIO13 (pin76) can be set as PIO13.
2. The PIO status during Power-On reset: PIO1, PIO10, PIO22, and PIO23 are input with pull-down, PIO4 to PIO9 are in normal operations, and the others are input with pull-up.

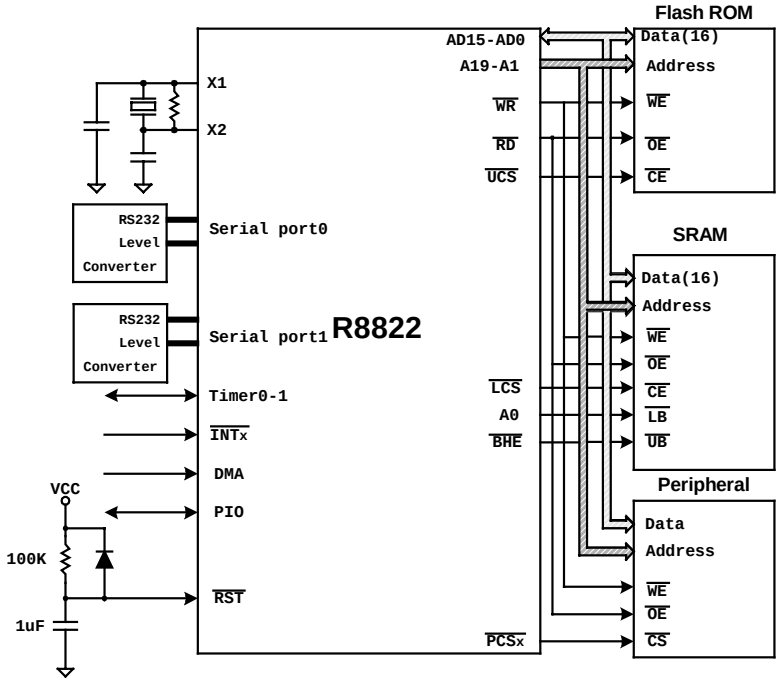
4.1 R8822 I/O Characteristics of Each Pin

PQFP Pin NO.	Pin Name	Characteristics
71	$\overline{RST}$	Schmitt Trigger input, with an internal 50K pull-up resistor
8	ARDY	Schmitt Trigger input, with an internal 50K pull-down resistor
45 47	HOLD NMI	CMOS input, with an internal 50K pull-down resistor
56 55	INT0 INT1/$\overline{SELECT}$	Schmitt Trigger TTL input, with an internal 10K pull-down resistor
16 17	CLKOUTA CLKOUTB	8mA 3-State CMOS output
9	$\overline{S2}$ /BWSEL	Bi-directional I/O, with a 50 K internal pull-up resistor 4mA TTL output
10 11	$\overline{S1}$ $\overline{S0}$	4mA 3-State CMOS output
43 6 5	$\overline{WLB}$ $\overline{RD}$ $\overline{WR}$	12mA 3-State CMOS output
19 20 22	A19/PIO9 A18/PIO8 A17/MA8/PIO7	Bi-directional I/O, with an enabled/disabled 10K internal pull-up resistors when functions as PIO. For normal function, the 10k pull-up resistor is disabled. 16mA TTL output

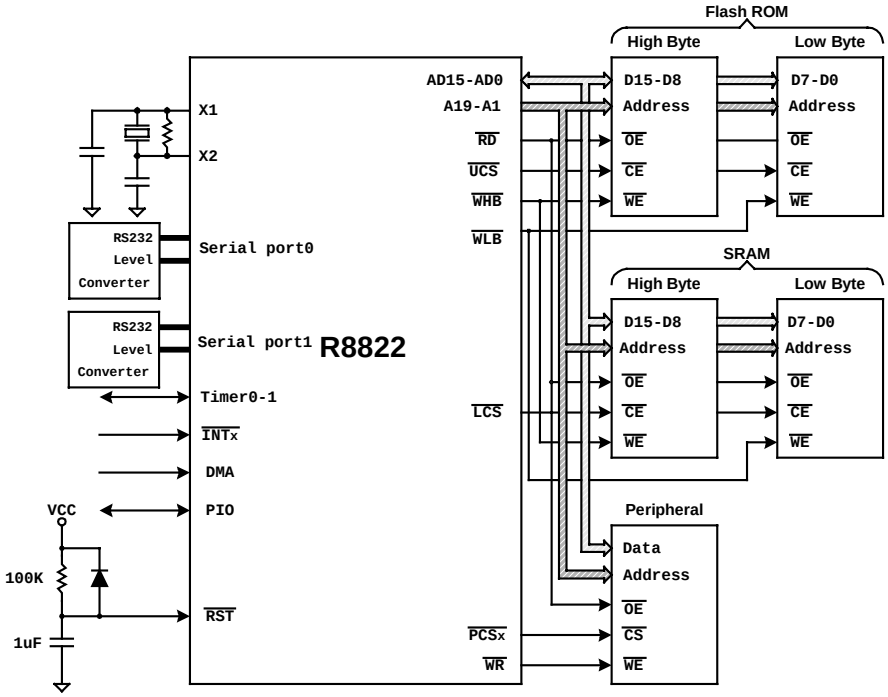
PQFP Pin NO.	Pin Name	Characteristics
23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 39 40	A16 A15/MA7 A14 A13/MA6 A12 A11/MA5 A10 A9/MA4 A8 A7/MA3 A6 A5/MA2 A4 A3/MA1 A2 A1/MA0 A0	16mA 3-State CMOS output
78 80 82 84 86 88 91 94 79 81 83 85 87 90 93 95	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15	Bi-directional I/O, 16mA TTL output
7	ALE	Bi-directional I/O, with a 50K internal pull-down resistor 4mA TTL output
46 74 73 2 1	SRDY/PIO6 TMROUT0/PIO10 TMROUT1/PIO1 TXD0/PIO22 RXD0/PIO23	Bi-directional I/O, with an enabled/disabled 10K internal pull-down resistor when functions as PIO. For normal function, the 10k pull-down resistor is disabled. 8mA TTL output
4	$\overline{\text{BHE}}$/$\overline{\text{ADEN}}$	Bi-directional I/O, with a 50 K internal pull-up resistor 4mA TTL output
42	$\overline{\text{WHB}}$	Bi-directional I/O, with a 50 K internal pull-up resistor 12mA TTL output
44	HLDA	4mA CMOS output
54 52	INT2/$\overline{\text{INTA0}}$/PIO31 INT4/PIO30	Bi-directional I/O, with an enabled/disabled 10 K internal pull-up resistor when functions as PIO. For normal function, the 10k pull-up resistor is disabled. 8mA TTL output, TTL Schmitt Trigger input
53	INT3/$\overline{\text{INTA1}}$/IRQ	Bi-directional I/O, with a 10 K internal pull-up resistor 8mA TTL output, TTL Schmitt Trigger input

PQFP Pin NO.	Pin Name	Characteristics
57 58	$\overline{UCS}$/$\overline{ONCE1}$ $\overline{LCS}$/$\overline{ONCE0}$/$\overline{RAS0}$	Bi-directional I/O, with a 10 K internal pull-up resistor 8mA TTL output, TTL Schmitt Trigger input
49 48 66 65 63 62 60 59 50 51 68 69 97 96 75 72 77 76 98 99 100 3	$\overline{DEN}$/PIO5 DT/$\overline{R}$/PIO4 $\overline{PCS0}$/PIO16 $\overline{PCS1}$/PIO17 $\overline{PCS2}$/$\overline{CTS1}$/$\overline{ENRX1}$/PIO18 $\overline{PCS3}$/$\overline{RTS1}$/$\overline{RTR1}$/PIO19 $\overline{PCS5}$/A1/PIO3 $\overline{PCS6}$/A2/PIO2 $\overline{MCS0}$/PIO14 $\overline{MCS1}$/$\overline{UCAS}$/PIO15 $\overline{MCS2}$/$\overline{LCAS}$/PIO24 $\overline{MCS3}$/$\overline{RAS1}$/PIO25 $\overline{UZI}$/PIO26 S6/$\overline{CLKDIV2}$/PIO29 TMRIN0/PIO11 TMRIN1/PIO0 DRQ0/INT5/PIO12 DRQ1/INT6/PIO13 TXD1/PIO27 RXD1/PIO28 $\overline{CTS0}$/$\overline{ENRX0}$/PIO21 $\overline{RTS0}$/$\overline{RTR0}$/PIO20	Bi-directional I/O, with an enabled/disabled 10 K internal pull-up resistor when functions as PIO. For normal function, the 10k pull-up resistor is disabled. 8mA TTL output

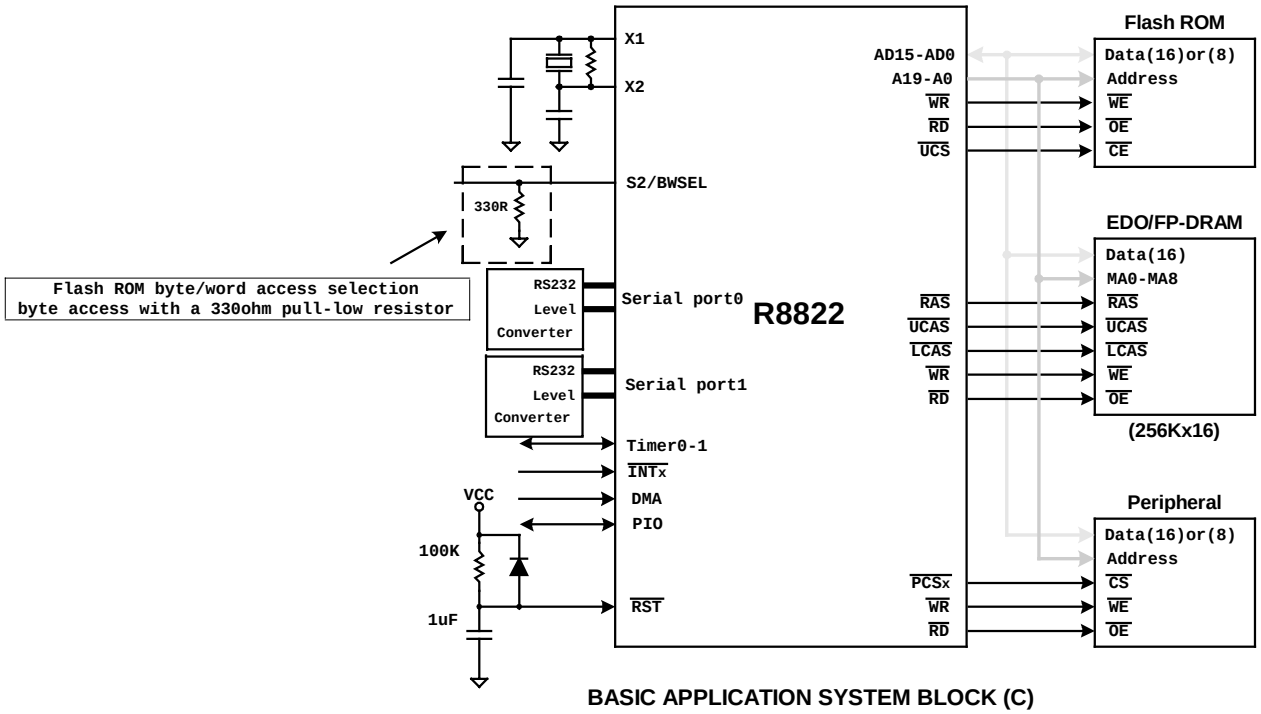
5. Basic Application System Block



BASIC APPLICATION SYSTEM BLOCK (A)

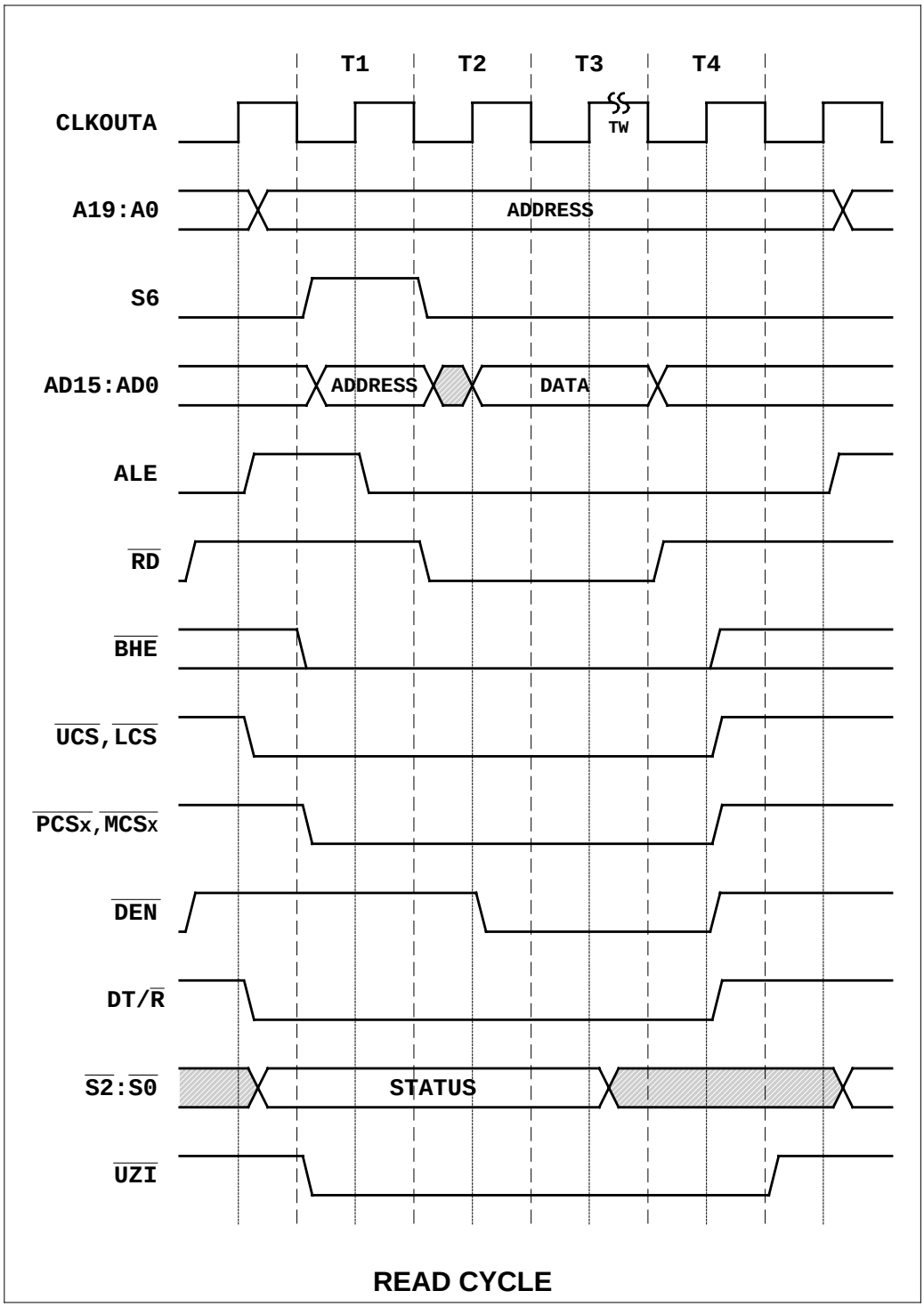


BASIC APPLICATION SYSTEM BLOCK (B)

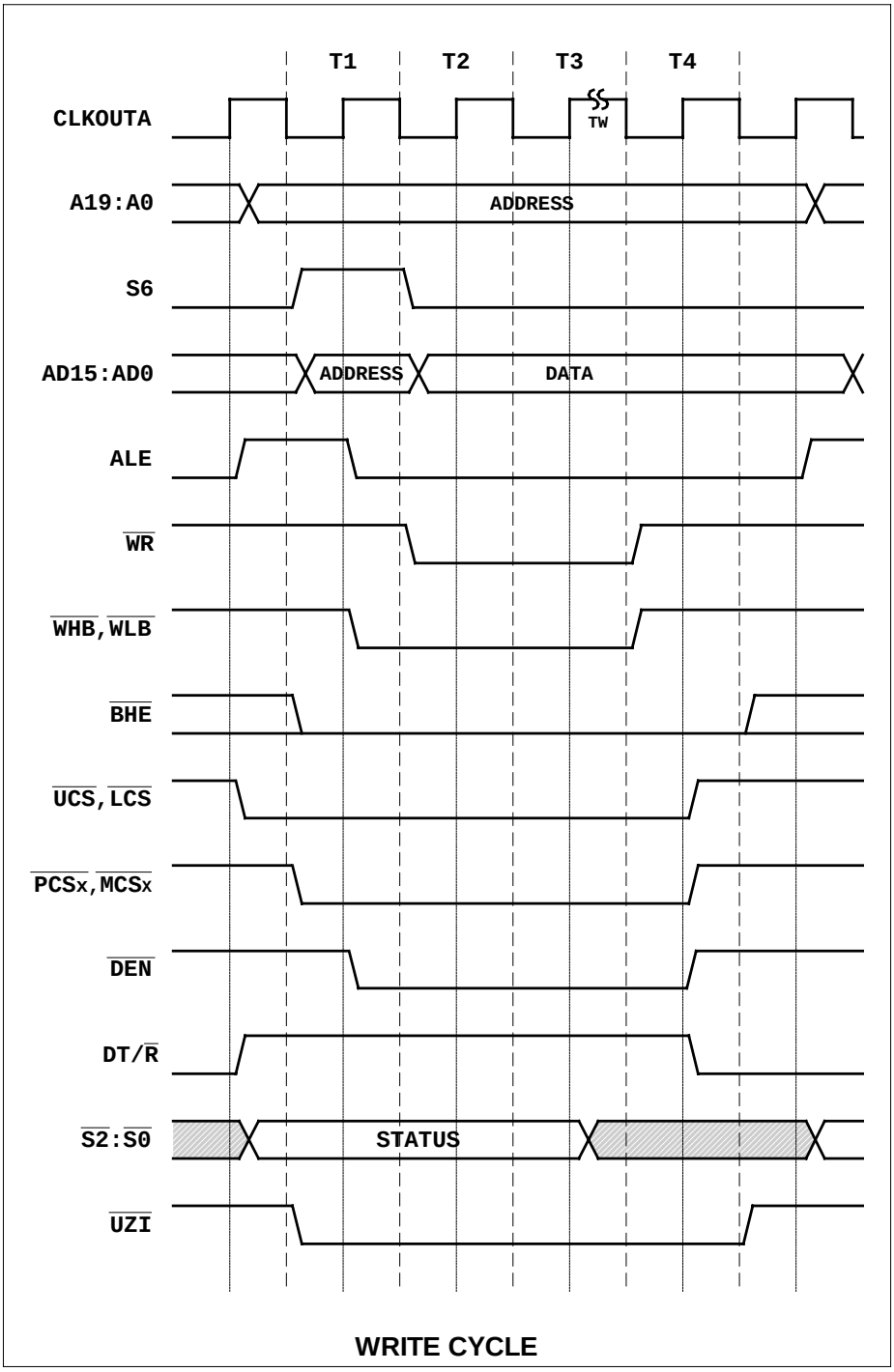


BASIC APPLICATION SYSTEM BLOCK (C)

6. Read/Write Timing Diagram

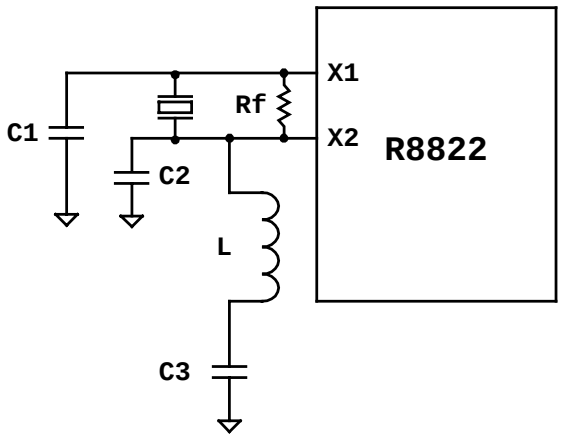


READ CYCLE


T1
T2
T3
T4
TW
CLKOUTA
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB,WLB
BHE
UCS,LCS
PCSx,MCSx
DEN
DT/R
S2:S0
STATUS
UZI

WRITE CYCLE

7. Crystal Characteristics



For fundamental-mode crystal:

Reference values

Frequency	10.8288MHz	19.66MHz	30MHz	33MHz	40MHz
Rf	None	None	None	None	None
C1	10Pf	10Pf	None	None	None
C2	10Pf	10Pf	10Pf	10Pf	10Pf
C3	None	None	None	None	None
L	None	None	None	None	None

For third-overtone mode crystal:

Reference values

Frequency	22.1184MHz	28.322MHz	33.177MHz	40MHz
Rf	1M	1.5M	1.5M	1.5M
C1	15Pf	15Pf	15Pf	15Pf
C2	30Pf	30Pf	30Pf	30Pf
C3	None	220Pf	220Pf	220Pf
L	None	10uL	4.7uL	2.7uL

8. Execution Unit

8.1 General Registers

The R8822 has eight 16-bit general registers. And the AX, BX, CX and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH and DL). The functions of these registers are described as follows.

AX: Word Divide, Word Multiply, Word I/O operation.

AL: Byte Divide, Byte Multiply, Byte I/O, Decimal Arithmetic, Translate operation.

AH: Byte Divide, Byte Multiply operation.

BX: Translate operation.

CX: Loops, String operation.

CL: Variable Shift and Rotate operation.

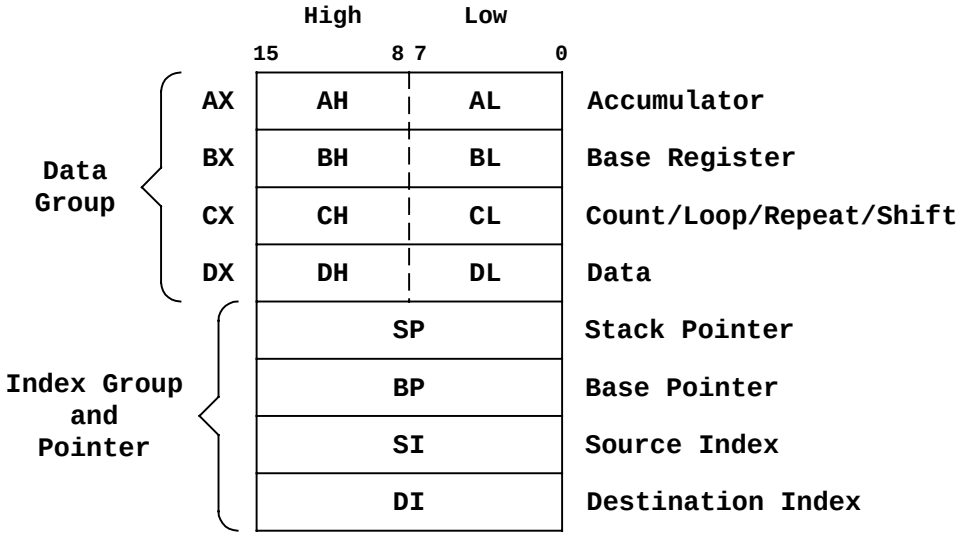
DX: Word Divide, Word Multiply, Indirect I/O operation

SP: Stack operations (POP, POPA, POPF, PUSH, PUSHA, PUSHF)

BP: General-purpose registers which can be used to determine offset address of operands in Memory.

SI: String operations

DI: String operations



GENERAL REGISTERS

8.2 Segment Registers

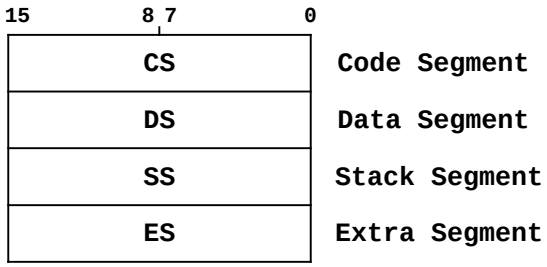
R8822 has four 16-bit segment registers, CS, DS, SS and ES. The segment registers contain the base addresses (starting location) of these memory segments, and they are immediately addressable for code (CS), data (DS & ES), and stack (SS) memory.

CS (Code Segment): The CS register points to the current code segment, which contains instruction to be fetched. The default location memory space for all instruction is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment): The DS register points to the current data segment, which generally contains program variables. The DS register is initialized to 0000H.

SS (Stack Segment): The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000H.

ES (Extra Segment): The ES register points to the current extra segment which is typically for data storage, such as large string operations and large data structures. The ES register is initialized to 0000H.



SEGMENT REGISTERS

8.3 Instruction Pointer and Status Flags Registers

IP (Instruction Pointer): The IP is a 16-bit register and it contains the offset of the next instruction to be fetched. The IP register cannot be directly accessed by software and is updated by the Bus Interface Unit. It can be changed, saved or restored as a result of program execution. The IP register is initialized to 0000H and the CS:IP starting execution address is at 0FFFF0H.

Processor Status Flags Registers **FLAGS**

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Res	AF	Res	PF	Res	CF

These flags reflect the status after the Execution Unit is executed.

Bit 15-12: Reserved

Bit 11: OF, Overflow Flag. If an arithmetic overflow occurs, this flag will be set.

Bit 10: DF, Direction Flag. If this flag is set, the string instructions are in the process of incrementing addresses. If DF is cleared, the string instructions are in the process of decrementing addresses. Refer to the STD and CLD instructions for setting and clearing the DF flag.

Bit 9: IF, Interrupt-Enable Flag. Refer to the STI and CLI instructions for setting and clearing the IF flag.

Set 1: The CPU enables the maskable interrupt request.

Set 0: The CPU disables the maskable interrupt request.

Bit 8: TF, Trace Flag. Set to enable single-step mode for debugging; cleared to disable the single-step mode. If an application program sets the TF flag with POPF or IRET instruction, a debug exception is generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.

Bit 7: SF, Sign Flag. If this flag is set, the high-order bit of the result of an operation will be 1,indicating the state of being negative.

Bit 6: ZF, Zero Flag. If this flag is set, the result of the operation will be zero.

Bit 5: Reserved

Bit 4: AF, Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low nibble of the AL general-purpose registers. It is used in BCD operation.

Bit 3: Reserved.

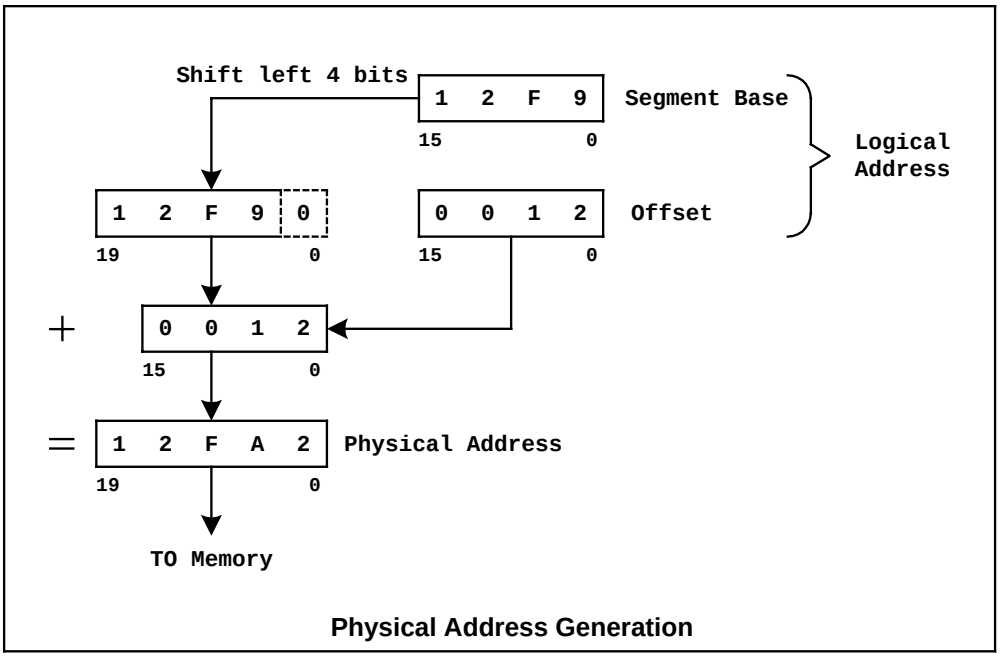
Bit 2: PF, Parity Flag. This flag will be set if the result of low-order 8-bit operation has even parity.

Bit 1: Reserved

Bit 0: CF, Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

8.4 Address Generation

The Execution Unit generates a 20-bit physical address to Bus Interface Unit by the Address Generation. Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



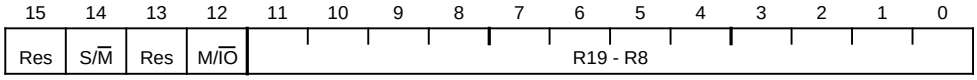
Physical Address Generation

9. Peripheral Control Block Registers

The peripheral control block can be mapped into either memory or I/O space by programming the FEh register. And it starts at FF00h in I/O space when the microprocessor is reset. The following table is the definitions of all the peripheral Control Block Registers, and the detailed descriptions will be arranged on the related Block Unit.

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	29	66	Timer 2 Mode / Control Register	74
FA	Disable Peripheral Clock Register	32	62	Timer 2 Maxcount Compare A Register	75
F6	Reset Configuration Register	34	60	Timer 2 Count Register	75
F4	Processor Release Level Register	29	5E	Timer 1 Mode / Control Register	73
F2	Auxiliary Configuration Register	39	5C	Timer 1 Maxcount Compare B Register	74
F0	Power-Save Control Register	31	5A	Timer 1 Maxcount Compare A Register	74
E6	Watchdog Timer Control Register	76	58	Timer 1 Count Register	74
E4	Refresh Counter Register	90	56	Timer 0 Mode / Control Register	71
E2	Refresh Reload Value Counter Register	90	54	Timer 0 Maxcount Compare B Register	73
DA	DMA 1 Control Register	67	52	Timer 0 Maxcount Compare A Register	73
D8	DMA 1 Transfer Count Register	67	50	Timer 0 Count Register	73
D6	DMA 1 Destination Address High Register	67	46	Power Down Configuration Register	32
D4	DMA 1 Destination Address Low Register	68	44	Serial Port 0 interrupt control register	50
D2	DMA 1 Source Address High Register	68	42	Serial port 1 interrupt control register	50
D0	DMA 1 Source Address Low Register	68	40	INT4 Control Register	51
CA	DMA 0 Control Register	64	3E	INT3 Control Register	51
C8	DMA 0 Transfer Count Register	66	3C	INT2 Control Register	52
C6	DMA 0 Destination Address High Register	66	3A	INT1 Control Register	53
C4	DMA 0 Destination Address Low Register	66	38	INT0 Control Register	53
C2	DMA 0 Source Address High Register	66	36	DMA 1/INT6 Interrupt Control Register	54
C0	DMA 0 Source Address Low Register	67	34	DMA 0/INT5 Interrupt Control Register	55
A8	$\overline{PCS}$ and $\overline{MCS}$ Auxiliary Register	43	32	Timer Interrupt Control Register	56
A6	Midrange Memory Chip Select Register	42	30	Interrupt Status Register	56
A4	Peripheral Chip Select Register	44	2E	Interrupt Request Register	57
A2	Low Memory Chip Select Register	41	2C	Interrupt In-service Register	58
A0	Upper Memory Chip Select Register	40	2A	Priority Mask Register	59
88	Serial Port 0 Baud Rate Divisor Register	83	28	Interrupt Mask Register	60
86	Serial Port 0 Receive Register	83	26	Poll Status Register	61
84	Serial Port 0 Transmit Register	83	24	Poll Register	61
82	Serial Port 0 Status Register	82	22	End-of-Interrupt Register	62
80	Serial Port 0 Control Register	80	20	Interrupt Vector Register	62
7A	PIO Data 1 Register	86	18	Serial port 1 baud rate divisor	84
78	PIO Direction 1 Register	86	16	Serial port 1 receive register	84
76	PIO Mode 1 Register	87	14	Serial port 1 transmit register	84
74	PIO Data 0 Register	87	12	Serial port 1 status register	84
72	PIO Direction 0 Register	87	10	Serial port 1 control register	84
70	PIO Mode 0 Register	88			

Peripheral Control Block Relocation Register: **Offset : FEh**
Reset Value : 20FFh



The peripheral control block is mapped into either memory or I/O space by programming this register. When the other chip selects ($\overline{PCSx}$ or $\overline{MCSx}$) are programmed to zero wait state and ignore the external ready, the $\overline{PCSx}$ or $\overline{MCSx}$ can overlap the control block.

Bit 15: Reserved

Bit 14: **S/$\overline{M}$** , Slave/Master – Configures the interrupt controller

S**et 0:** Master mode,

Set 1: Slaved mode

Bit 13: Reserved

Bit 12: **M/$\overline{IO}$** , Memory/IO space. At reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space.

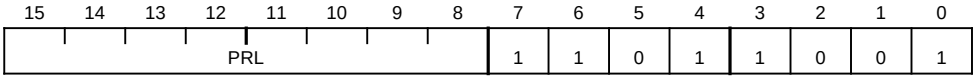
S**et 1:** The peripheral control block (PCB) is located in memory space.

S**et 0:** The PCB is located in I/O space.

Bit 11-0: **R19-R8**, Relocation Address Bits

The upper address bits of the PCB base address. The defaults of the lower eight bits are 00h. When the PCB is mapped to I/O space, the R19-R16 must be programmed to 0000b.

Processor Release Level Register **Offset : F4h**
Reset Value : —D9h



This read only register specifies the processor release version and RDC identification number

Bit 15-13: read only- 011**.**

Bit 12-8: Processor version

01h: version A, 02h: version B, 03h: version C, 04h: version D,

Bit 7-0: RDC identification number - D9h

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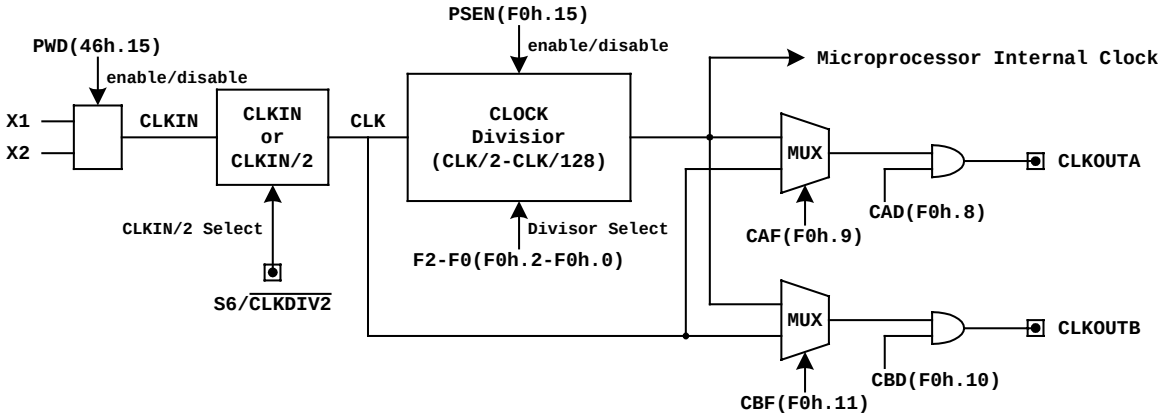
10. Power Save & Power Down



System Clock

The CPU provides power-save & power-down functions.

*** Power-Save:**

In power-save mode, users can program the Power-Save Control Register to divide the internal operating clock. Users can also disable each non-used peripheral clock by programming the Disable Peripheral Clock Register.

*** Power-Down:**

This CPU can enter power-down mode (stop clock) when the Power Down Configuration Register is programmed during the CPU running in full speed mode or power-save mode. The CPU will be waked up when each one of the external INT0, INT1, INT2, INT3, and INT4 pins is active high and the CPU operating clock will go back to full speed mode if the INT is serviced (the interrupt flag is enabled). If the interrupt flag is disabled, then the CPU will be waked up by the INT, the operating clock will go back to the previous operating clock state, and the CPU will execute the next program counter instruction. There is 19-bit counter time waiting the crystal clock stable when the CPU wakes up from stop clock mode.

Power-Save Control Register

Offset : F0h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSEN	MCSBIT	0	0	CBF	CBD	CAF	CAD	0	0	0	0	0	F2	F1	F0

Bit 15: **PSEN**, Enable Power-save Mode. This bit is cleared by hardware when an external interrupt occurs. This bit will not change when software interrupts (INT instruction) and exceptions occur.

Set 1: enable power-save mode and divide the internal operating clock by the value in F2-F0.

Bit14: MCSBIT, $\overline{\text{MCS0}}$ control bit.

Set 0: $\overline{\text{MCS0}}$ operates normally.

Set 1: $\overline{\text{MCS0}}$ is active over the entire $\overline{\text{MCSx}}$ range

Bit13-12: Reserved

Bit 11: **CBF**, CLKOUTB Output Frequency selection.

Set 1: CLKOUTB output frequency is the same as crystal input frequency.

Set 0: CLKOUTB output frequency is from the clock divisor, which frequency is the same as that of microprocessor internal clock.

Bit 10: CBD, CLKOUTB Drive Disable

Set 1: Disable the CLKOUTB. This pin will be three-stated.

Set 0: Enable the CLKOUTB.

Bit 9: CAF, CLKOUTA Output Frequency selection.

Set 1: CLKOUTA output frequency is the same as crystal input frequency.

Set 0: CLKOUTA output frequency is from the clock divisor, which frequency is the same as that of microprocessor internal clock.

Bit 8: CAD, CLKOUTA Drive Disable.

Set 1: Disable the CLKOUTA. This pin will be three-stated.

Set 0: Enable the CLKOUTA.

Bit 7-3: Reserved

Bit 2-0: F2- F0, Clock Divisor Select.

F2,	**F1,**	**F0**	-----	**Divider Factor**
0,	0,	0	----	Divided by 1
0,	0,	1	----	Divided by 2
0,	1,	0	----	Divided by 4
0,	1,	1	----	Divided by 8
1,	0,	0	----	Divided by 16
1,	0,	1	----	Divided by 32
1,	1,	0	----	Divided by 64
1,	1,	1	----	Divided by 128

Disable Peripheral Clock Register

Offset : FAh
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntClk	UART Clk	DMA Clk	Timer Clk	Reserved											

Bit 15: Int Clk. Set 1 to stop the Interrupt controller clock.

Bit 14: UART Clk. Set 1 to stop the asynchronous serial port controller clock.

Bit 13: DMA Clk. Set 1 to stop the DMA controller clock.

Bit 12: Timer Clk. Set 1 to stop the Timer controller clock.

Bit 11-0: Reserved

Power Down Configuration Register

Offset : 46h
Reset Value : 00h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWD	0	0	0	0	0	0	WIF	0	0	0	I4	I3	I2	I1	I0

Bit 15: PWD, Power-Down Enable. When this bit is set to 1, the CPU will enter power-down mode, then the crystal clock will stop. The CPU will be waked up when an external INT (INT0 – INT4) are active high. It will wait 19-bit counter time for the crystal clock to be stable before CPU is waked up.

Bit 14-9: Reserved

Bit 8: WIF, Wake-up Interrupt Flag. Read only bit. When the CPU is waked up by interrupt from power-down mode, this bit will be set to 1 by hardware. Otherwise this bit is 0.

Bit 7-5: Reserved

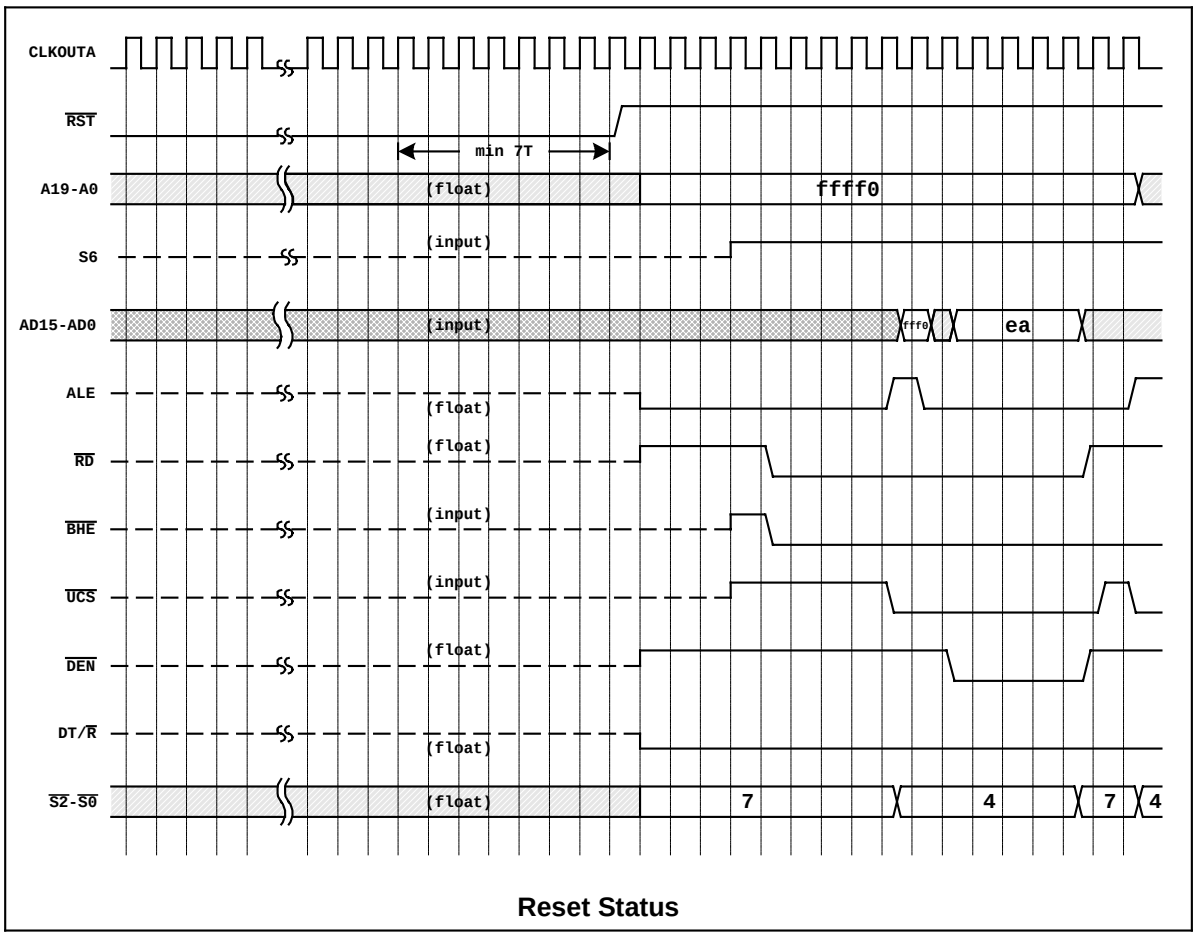
Bit 4 -0: **I4 -I0,** Enable the external interrupt (INT4 – INT0) wake-up function.

Set these bits to 1 to make the INT pins function as power-down wake up pins.

---

11. Reset

Processor initialization is accomplished with activation of the $\overline{RST}$ pin. To reset the processor, this pin should be held high for at least seven oscillator periods. The Reset Status Figure shows the status of the $\overline{RST}$ pin and other related pins. When $\overline{RST}$ goes from low to high, the state of input pins (with weakly pulled-up or pulled-down) will be latched, and each pin will perform the individual function. The AD15-AD0 will be latched into the register F6h. $\overline{UCS}$ / $\overline{ONCE1}$ and $\overline{LCS}$ / $\overline{ONCE0}$ / $\overline{RAS0}$ will enter ONCE mode (All of the pins will float except X1 and X2) when they are with pull-low resistors. The input clock will be divided by 2 when S6/ $\overline{CLKDIV2}$ is with a pull-low resistor. The AD15-AD0 bus will drive both of the address and data regardless of the DA bit setting during $\overline{UCS}$ and $\overline{LCS}$ cycles if $\overline{BHE}$ / $\overline{ADEN}$ is with a pull-low resistor

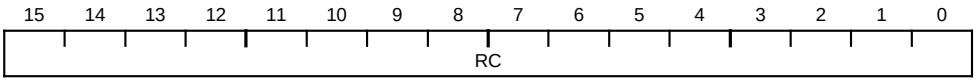


Reset Status

Reset Configuration Register

Offset : F6h

Reset Value : AD15-AD0



Bit 15- 0: **RC**, Reset Configuration AD15 – AD0.

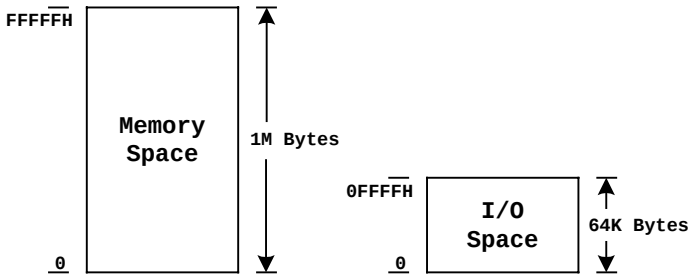
The AD15 to AD0 must be with weakly pulled-up or pulled-down resistors to correspond to the contents when AD15-AD0 are latched into this register during the $\overline{\text{RST}}$ pin goes from low to high. The value of the reset configuration register provides the system information when this register is read by software This register is read only and the contents remain valid until next processor reset.

12. Bus Interface Unit

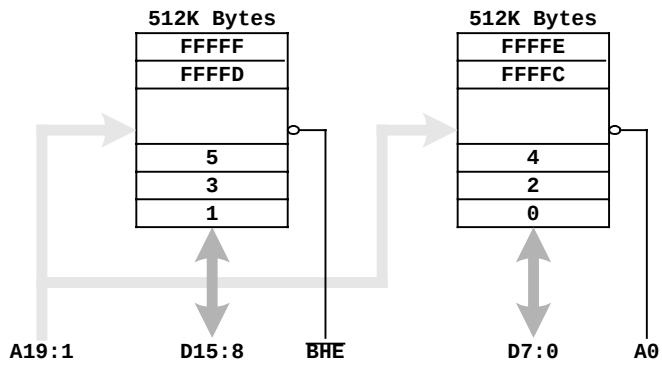
The bus interface unit drives address, data, status and control information to define a bus cycle. The bus A19-A0 are non-multiplexed memory or I/O addresses. The AD15-AD0 are multiplexed addresses and data bus for memory or I/O accessing. The $\overline{S2}$ - $\overline{S0}$ are encoded to indicate the bus status, which is described in the Pin Description table (page 12). The Basic Application System Block (page 19) and Read/Write Timing Diagram (page 21) describe the basic bus operations. When the DRAM controller is enabled, AD15-AD0 will perform the DRAM data bus during microcontroller accessing DRAM. And the MA8-MA0 are multiplexed with Address bus.

12.1 Memory and I/O Interface

The memory space consists of 1M bytes (512k 16-bit port) and the I/O space consists of 64k bytes (32k 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instruction can access I/O address space, and information must be transferred between the peripheral device and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64k bytes I/O address space can be accessed indirectly, through the DX register. I/O instructions always force address A19-A16 to low level.



Memory and I/O Space



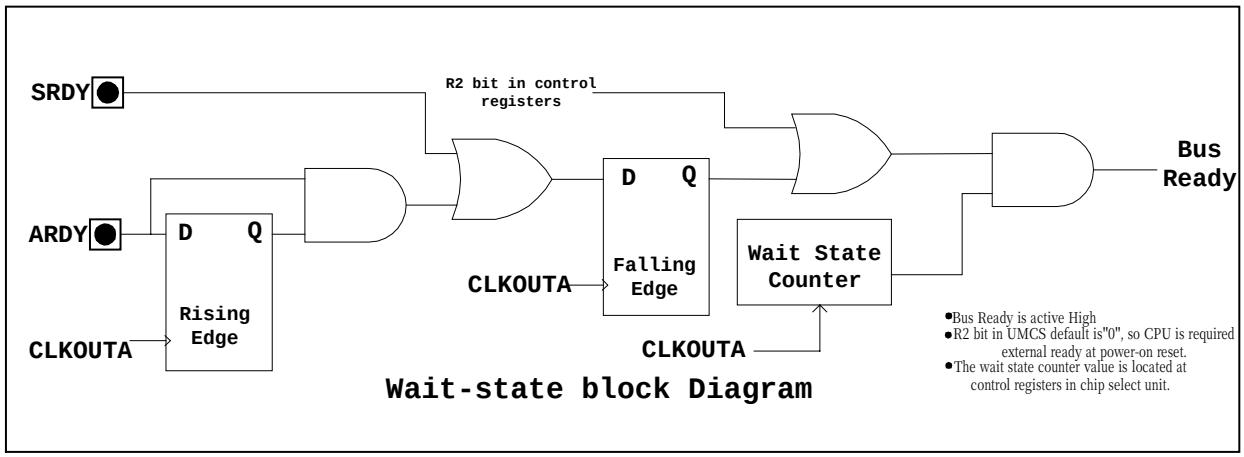
Physical Data Bus Models

12.2 Data Bus

The memory address space data bus is physically implemented by dividing the address space into two banks of up to 512k bytes. One bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0), the other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). A0 and $\overline{BHE}$ determine whether one bank or both banks participate in the data transfer.

12.3 Wait States

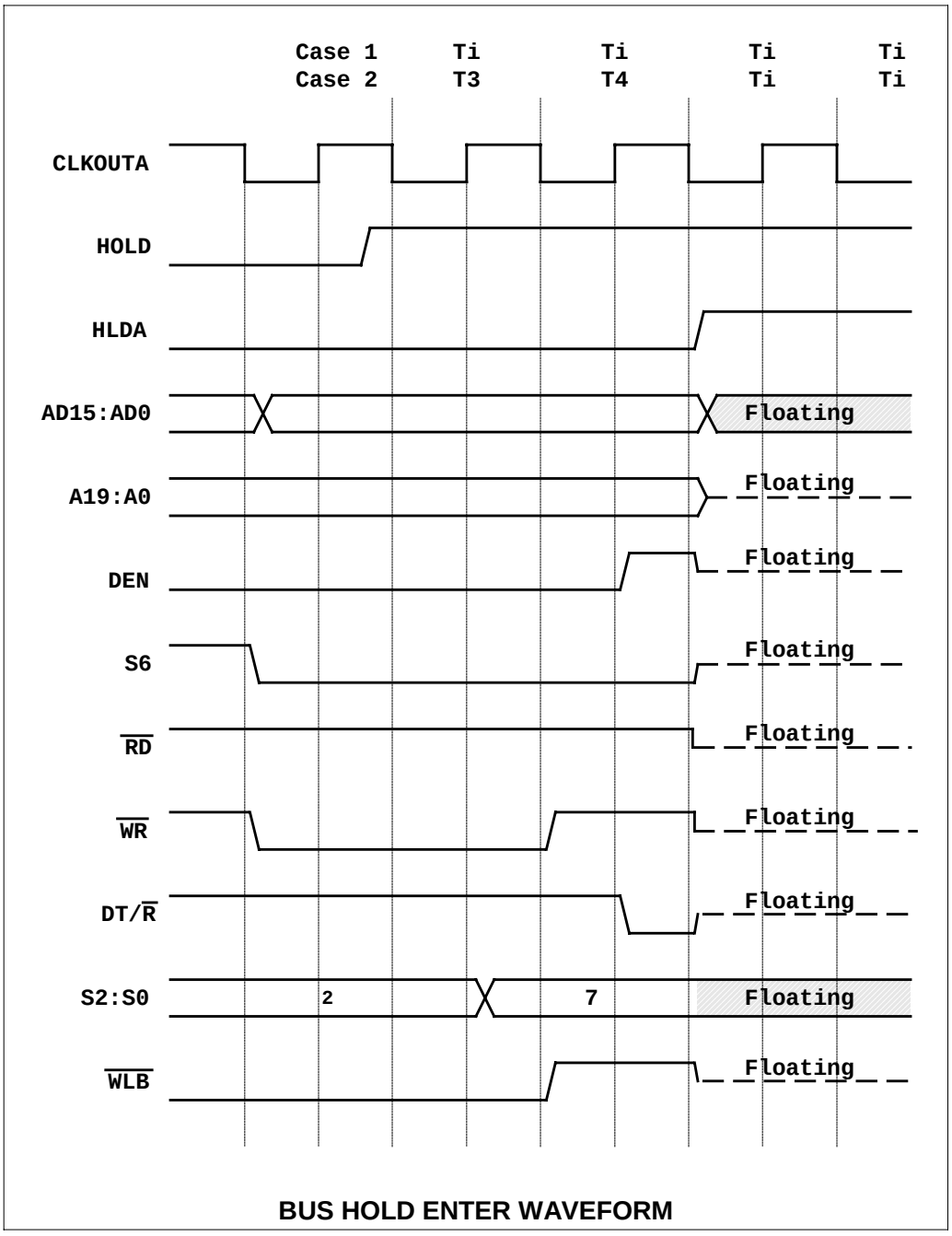
Wait states extend the data phase of the bus cycle. The ARDY or SRDY input with low level will be inserted wait states in. If R2 bit =0, the user can also insert wait states by programming the internal chip select registers. The R2 bit of UMCS (offset 0A0h) default is low, so either ARDY or SRDY should be in ready state (with pull-high resistors) when at power on reset or external reset. The wait state counter value is decided by the R3, R1and R0 bits in each chip select register. There are five groups of R3, R1 and R0 bits in the registers offset A0h, A2h, A4h, A6h and A8h. Each group is independent.



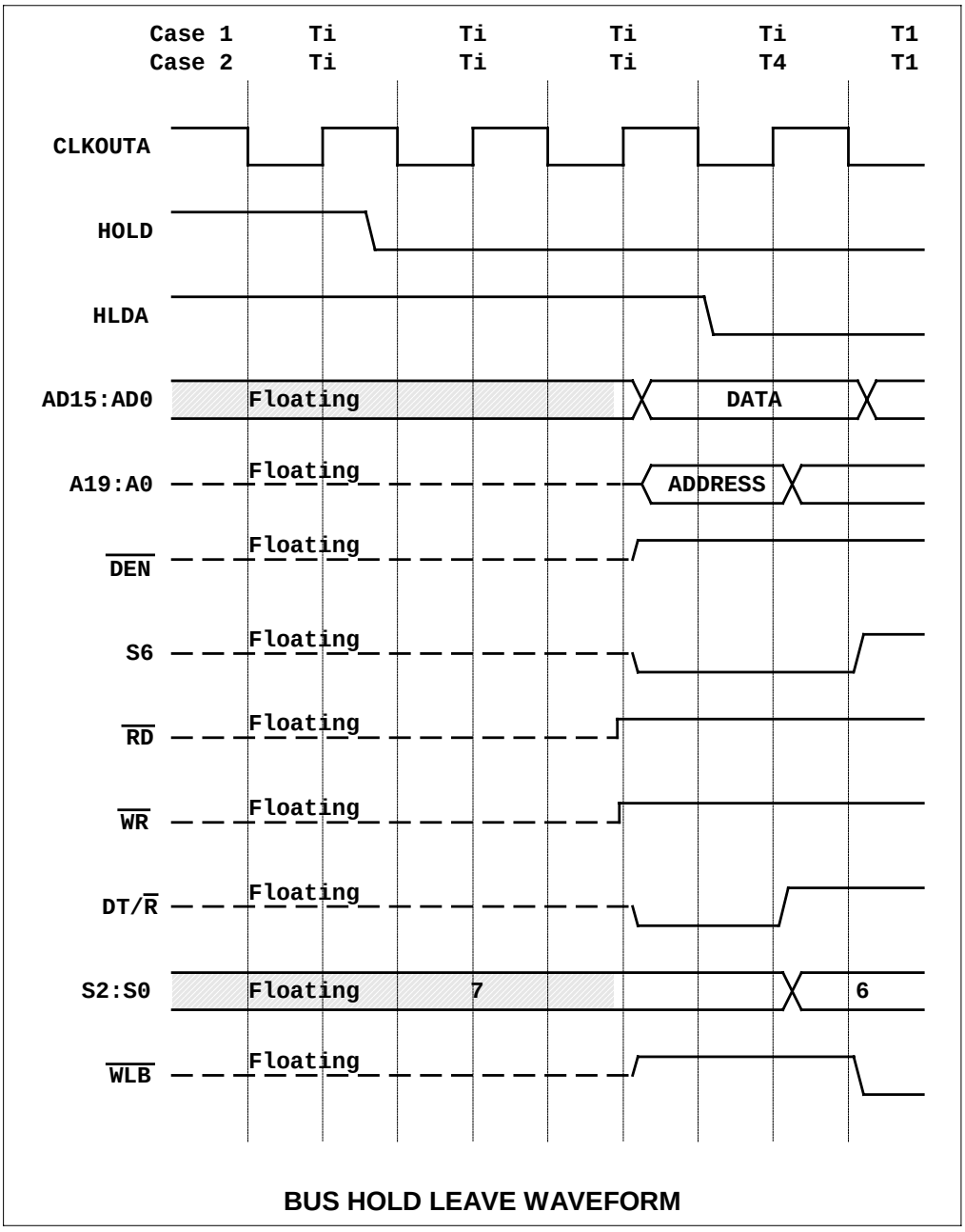
Wait-state block Diagram

12.4 Bus Hold

When the bus hold is requested (HOLD pin and active high) by another bus master, the microprocessor will issue a HLDA in response to a HOLD request at the end of T4 or Ti. When the microprocessor is in hold status (HLDA is high), the AD15-AD0, A19-A0, $\overline{WR}$, $\overline{RD}$, $\overline{DEN}$, $\overline{SI}$ - $\overline{S0}$, S6, $\overline{BHE}$, DT/$\overline{R}$, $\overline{WHB}$ and $\overline{WLB}$ are floating, and the $\overline{UCS}$, $\overline{LCS}$, $\overline{PCS6}$ - $\overline{PCS5}$, $\overline{MCS3}$ - $\overline{MCS0}$ and $\overline{PCS3}$ - $\overline{PCS0}$ will be driven high. After HOLD is detected as being low, the microprocessor will lower the HLDA.



BUS HOLD ENTER WAVEFORM



BUS HOLD LEAVE WAVEFORM

12.5 Bus Width

The R8822 default is 16-bit bus access and the bus can be programmed as 8-bit or 16-bit access when memory or I/O access is located in the $\overline{\text{LCS}}$, $\overline{\text{MCSx}}$ or $\overline{\text{PCSx}}$ address space. The $\overline{\text{UCS}}$ code- fetched selection can be 8-bit or 16-bit bus width, which is decided by the $\overline{\text{S2}}$/BWSEL pin input status as the $\overline{\text{RST}}$ pin goes from low to high. When the $\overline{\text{S2}}$/BWSEL pin is with a pull-low resistor, the code- fetched selection is 8-bit bus width. The DRAM bus width is 16 bits, which cannot be changed.

Auxiliary Configuration Register

Offset : F2h

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								USIZ	ENRX1	RTS1	ENRX0	RTS0	LSIZ	MSIZ	IOSIZ

Bit 15-8: Reserved.

Bit 7:**USIZ**, Boot code bus width. This bit reflects the $\overline{S2}$ /BWSEL pin input status when $\overline{RST}$ pin goes from low to high.

Set 0: 16-bit bus width booting when $\overline{S2}$ /BWSEL pin is without a pull-low resistor.

Set 1: 8-bit bus width booting when $\overline{S2}$ /BWSEL pin is with a 330 ohm pull-low resistor.

Bit 6: ENRX1, Enable the Receiver Request of Serial port 1.

Set 1: The $\overline{CTS1}$ / $\overline{ENRX1}$ pin is configured as $\overline{ENRX1}$

Set 0: The $\overline{CTS1}$ / $\overline{ENRX1}$ pin is configured as $\overline{CTS1}$

Bit 5: RTS1, Enable Request to Send of Serial port 1.

Set 1: The $\overline{RTR1}$ / $\overline{RTS1}$ pin is configured as $\overline{RTS1}$

Set 0: The $\overline{RTR1}$ / $\overline{RTS1}$ pin is configured as $\overline{RTR1}$

Bit 4: ENRX0, Enable the Receiver Request of Serial port 0.

Set 1: The $\overline{CTS0}$ / $\overline{ENRX0}$ pin is configured as $\overline{ENRX0}$

Set 0: The $\overline{CTS0}$ / $\overline{ENRX0}$ pin is configured as $\overline{CTS0}$

Bit 3: RTS0, Enable Request to Send of Serial port 0.

Set 1: The $\overline{RTR0}$ / $\overline{RTS0}$ pin is configured as $\overline{RTS0}$

Set 0: The $\overline{RTR0}$ / $\overline{RTS0}$ pin is configured as $\overline{RTR0}$

Bit 2: LSIZ, $\overline{LCS}$ Data Bus Size selection. This bit cannot be changed while it is executed from the $\overline{LCS}$ space or while the Peripheral Control Block is overlaid with $\overline{PCS}$ space.

Set 1: 8-bit data bus access when the memory access is located in the $\overline{LCS}$ memory space.

Set 0: 16-bit data bus access when the memory access is located in the $\overline{LCS}$ memory space.

Bit 1: MSIZ, $\overline{MCSx}$ and $\overline{PCSx}$ Memory Data Bus Size selection. This bit cannot be changed while it is executed from the associated address space or while the Peripheral Control Block is overlaid on this address space.

Set 1: 8-bit data bus access when the memory access is located in the selection memory space.

Set 0: 16-bit data bus access when the memory access is located in the selection memory space.

Bit 0: IOSIZ, I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses.

Set 1: 8-bit data bus access.

Set 0: 16-bit data bus access.

13. Chip Select Unit

The Chip Select Unit provides 12 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through five peripheral control registers (A0h, A2h, A4h, A6h, A8h) and all the chip selects can be inserted wait states in by programming the peripheral control register.

13.1 $\overline{\text{UCS}}$

The $\overline{\text{UCS}}$ default is active on reset for code access. The memory active range is upper 512k (80000h – FFFFFh), which is programmable. And the default memory active range of $\overline{\text{UCS}}$ is 64k (F0000h – FFFFFh). The $\overline{\text{UCS}}$ is active to drive low four CLKOUTA oscillators if no wait state is inserted. There are three wait-states inserted into $\overline{\text{UCS}}$ active cycle on reset.

Upper Memory Chip Select Register

Offset : A0h

Reset Value :F03Bh

15	14 13 12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB2 - LB0	0	0	0	0	DA	UDEN	1	1	1	R2	R1	R0

Bit 15: Reserved

Bit 14-12: LB2-LB0, Memory block size selection for $\overline{\text{UCS}}$ chip select pin.

The active range of the $\overline{\text{UCS}}$ chip select pin can be configured by the LB2-LB0.

The default memory block size is from F0000h to FFFFFh.

LB2, LB1, LB0 ---- Memory Block size , Start address, End Address

1 , 1 , 1 ---- 64k , F0000h , FFFFFh

1 , 1 , 0 ---- 128k , E0000h , FFFFFh

1 , 0 , 0 ---- 256k , C0000h , FFFFFh

0 , 0 , 0 ---- 512k , 80000h , FFFFFh

Bit 11-8: Reserved

Bit 7: DA, Disable Address. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held low on the rising edge of $\overline{\text{RST}}$, the AD bus always drives the address and data.

Set 1: Disable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted.

Set 0: Enable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{UCS}}$ is asserted.

Bit 6: UDEN, Upper DRAM Enable. Set this bit to enable the bank2 (80000h – FFFFFh) DRAM controller. When the UDEN is set, the $\overline{\text{MCS3}}$ pin becomes $\overline{\text{RAS1}}$, and the $\overline{\text{MCS1}}$ and $\overline{\text{MCS2}}$ pins become $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ respectively. The $\overline{\text{UCS}}$ pin is disabled when the UDEN bit is set to 1. Users can boot the code from flash memory with $\overline{\text{UCS}}$ pin, and switch space to a DRAM bank 1 after system initialization.

Bit 5-3: Reserved

Bit 2: R2, Ready Mode. This bit is used to configure the ready mode for $\overline{\text{UCS}}$ chip select.

Set 1: external ready is ignored.

Set 0: external ready is required.

Bit 1-0: R1-R0, Wait-State value. When R2 is set to 0, it can insert wait-states into an access to the $\overline{\text{UCS}}$ memory area. The reset value of (R1,R0) is (1,1).

(R1,R0) = (0,0) -- 0 wait-state ; (R1,R0) = (0,1) -- 1 wait-state

(R1,R0) = (1,0) -- 2 wait-states ; (R1,R0) = (1,1) -- 3 wait-states

---

13.2 $\overline{\text{LCS}}$

The lower 512k bytes (00000h-7FFFFh) memory region chip selects. The memory active range is programmable, which has no default size on reset. So the A2h register must be programmed first before accessing the target memory range. The $\overline{\text{LCS}}$ pin is not active on reset, but any read or write access to the A2h register activates this pin.

Low Memory Chip Select Register

Offset : A2h

Reset Value : —

15	14 13 12	11	10	9	8	7	6	5	4	3	2	1	0
0	UB2 - UB0	1	1	1	1	DA	LDEN	1	1	1	R2	R1	R0

Bit 15: Reserved

Bit 14-12: UB2-UB0, Memory block size selection for $\overline{\text{LCS}}$ chip select pin

The active range of the $\overline{\text{LCS}}$ chip select pin can be configured by UB2-UB0.

The $\overline{\text{LCS}}$ pin is not active on reset, but any read or write access to the A2h (LMCS) register activates this pin.

UB2, UB1, UB0 ---- Memory Block size , Start address, End Address

0 ,	0 ,	0	----	64k	, 00000h	, 0FFFFh
0 ,	0 ,	1	----	128k	, 00000h	, 1FFFFh
0 ,	1 ,	1	----	256k	, 00000h	, 3FFFFh
1 ,	1 ,	1	----	512k	, 00000h	, 7FFFFh

Bit 11-8: Reserved

Bit 7: DA, Disable Address. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held high on the rising edge of $\overline{\text{RST}}$, the DA bit is valid to enable/disable the address phase of the AD bus. If the $\overline{\text{BHE}}$ / $\overline{\text{ADEN}}$ pin is held low on the rising edge of $\overline{\text{RST}}$, the AD bus always drives the address and data.

Set 1: Disable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{LCS}}$ is asserted.

Set 0: Enable the address phase of the AD15 – AD0 bus cycle when $\overline{\text{LCS}}$ is asserted.

Bit 6: LDEN, Lower DRAM Enable. This bit is used to enable the bank 0 (00000h-7FFFFh) DRAM controller.

Set LDEN to 1, the $\overline{\text{LCS}}$ pin becomes $\overline{\text{RAS0}}$, and the $\overline{\text{MCS1}}$ and $\overline{\text{MCS2}}$ pins become $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$

respectively.

Bit 5-3: Reserved

Bit 2: R2, Ready Mode. This bit is used to configure the ready mode for $\overline{LCS}$ chip select.

Set 1: external ready is ignored.

Set 0: external ready is required.

Bit 1-0: R1-R0, Wait-State value. When R2 is set to 0, it can insert wait-states into an access to the $\overline{LCS}$ memory area.

(R1,R0) = (0,0) -- 0 wait-state ; (R1,R0) = (0,1) -- 1 wait-state

(R1,R0) = (1,0) -- 2 wait-states ; (R1,R0) = (1,1) -- 3 wait-states

---

13.3 $\overline{MCSx}$

The memory block of $\overline{MCS3}$ - $\overline{MCS0}$ can be located anywhere within the 1M-byte memory space, exclusive of the areas associated with the $\overline{UCS}$ and $\overline{LCS}$ chip selects. The maximum $\overline{MCSx}$ active memory range is 512k bytes. The 512k $\overline{MCSx}$ block size can only be used when located at address 00000h, and the $\overline{LCS}$ chip selects must not be active in this case. Locating a 512k $\overline{MCSx}$ block size at 80000h always conflicts with the range of $\overline{UCS}$ or $\overline{RAS1}$ and is not allowed. The $\overline{MCSx}$ chip selects are programmed through two registers A6h and A8h, and these select pins are not active on reset. Both A6h and A8h registers must be accessed with a read or write to activate $\overline{MCS3}$ - $\overline{MCS0}$. There aren't default values on A6h and A8h registers, so the A6h and A8h must be programmed first before $\overline{MCS3}$ - $\overline{MCS0}$ are active. When the DRAM controller is enabled, the $\overline{MCS3}$ - $\overline{MCS1}$ are performed as DRAM interface. (Refer to the DRAM controller unit)

Midranage Memory Chip Select Register

Offset : A6h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA19 - BA13							1	1	1	1	1	1	R2	R1	R0

Bit 15-9: BA19-BA13, Base Address. The BA19-BA13 correspond to bits 19-13 of the 1M-bytes (20-bits) programmable base address of the $\overline{MCS}$ chip select block. The bits 12 to 0 of the base address are always 0. The base address can be set to any integer multiple of the size of the memory block size selected in these bits. For example, if the midrange block is 32Kbytes, only the bits BA19 to BA15 can be programmed. So the block address could be located at 20000h or 38000h but not in 22000h. The base address of the $\overline{MCS}$ chip select can be set to 00000h only if the $\overline{LCS}$ chip select is not active. And the $\overline{MCS}$ chip select address range is not allowed to overlap the $\overline{LCS}$ chip select address range. The $\overline{MCS}$ chip select address range also is not allowed to overlap the $\overline{UCS}$ chip select address range.

Bit 8-3: Reserved

Bit 2: R2, Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{MCS}$ chip selects. The R1 andR0 bits of this register determine the number of wait states to be inserted.

Set 1: external ready is ignored

Set 0: external ready is required

Bit 1-0: R1-R0, Wait-State value. The R1 and R0 determine the number of wait states inserted into an $\overline{MCS}$ access.

(R1,R0) : (1,1) – 3 wait states , (1,0) – 2 wait states, (0,1) – 1 wait state , (0,0) – 0 wait state

---

$\overline{PCS}$ and $\overline{MCS}$ Auxiliary Register

Offset : A8h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	M6-M0							EX	MS	Reserved			R2	R1	R0

Bit 15: Reserved

Bit 14-8: M6-M0, $\overline{MCS}$ Block Size. These bits determine the total block size for the $\overline{MCS3}$ - $\overline{MCS0}$ chip selects. Each individual chip select is active for one quarter of the total block size. For example, if the block size is 32K bytes and the base address is located at 20000h, the individual active memory address range of $\overline{MCS3}$ to $\overline{MCS0}$ is $\overline{MCS0}$ – 20000h to 21FFF, $\overline{MCS1}$ -22000 to 23FFFh, $\overline{MCS2}$ - 24000h to 25FFFh, $\overline{MCS3}$ - 26000h to 27FFFh.

$\overline{MCSx}$ total block size is defined by M6-M0,

M6-M0	**Total block size**	$\overline{MCSx}$ **address active range**
0000001b	8k	2k
0000010b	16k	4k
0000100b	32k	8k
0001000b	64k	16k
0010000b	128k	32k
0100000b	256k	64k
1000000b	512k	128k

Bit 7: EX, Pin Selector. This bit configures the multiplexed output which the $\overline{PCS6}$ - $\overline{PCS5}$ pins as chip selects or A2-A1.

Set 1: $\overline{PCS6}$ and $\overline{PCS5}$ are configured as peripheral chip select pins.

Set 0: $\overline{PCS6}$ is configured as address bit A2 and $\overline{PCS5}$ is configured as A1.

Bit 6: MS, Memory or I/O space Selector.

Set 1: The $\overline{PCSx}$ pins are active for memory bus cycle.

Set 0: The $\overline{PCSx}$ pins are active for I/O bus cycle.

Bit 5-3: Reserved

Bit 2: R2, Ready Mode. This bit is configured to enable/disable the wait states inserted for the PCS5, PCS6 chip selects. The R1 and R0 bits of this register determine the number of wait state to insert.

Set 1: external ready is ignored

Set 0: external ready is required

Bit 1-0: R1-R0, Wait-State value. The R1 and R0 determine the number of wait states inserted into a $\overline{PCS5}$ - $\overline{PCS6}$ access.

(R1,R0) : (1,1) – 3 wait states , (1,0) – 2 wait states, (0,1) – 1 wait state , (0,0) – 0 wait state

13.4 PCSx

In order to define these pins, the peripheral or memory chip selects are programmed through A4h and A8h register. The base address memory block can be located anywhere within the 1M-byte memory space, exclusive of the areas associated with the UCS, LCS and MCS chip selects. If the chip selects are mapped to I/O space, the access range is 64k bytes. PCS6 – PCS5 can be configured from 0 wait-state to 3 wait-states. PCS3 – PCS0 can be configured from 0 wait-state to 15 wait-states.

Peripheral Chip Select Register

Offset : A4h

Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA19 - BA11									1	1	1	R3	R2	R1	R0

Bit 15-7: BA19-BA11, Base Address. BA19-BA11 correspond to bit 19-11 of the 1M-byte (20 bits) programmable base address of the PCS chip select block. When the PCS chip selects are mapped to I/O space, BA19-BA16 must be written to 0000b because the I/O address bus is only 64K bytes (16-bits) wide.

PCSx address range:

PCS0	:	Base Address	-	Base Address+255
PCS1	:	Base Address+256	-	Base Address+511
PCS2	:	Base Address+512	-	Base Address+767
PCS3	:	Base Address+768	-	Base Address+1023
PCS5	:	Base Address+1280	-	Base Address+1535
PCS6	:	Base Address+1536	-	Base Address+1791

Bit 6-4: Reserved

Bit 3: R3; **Bit 1-0: R1, R0** ,Wait-State Value. The R3, R1 and R0 determine the number of wait-states inserted into a PCS3 - PCS0 access.

R3,	R1,	R0	--	Wait States
0,	0,	0	--	0
0,	0,	1	--	1
0,	1,	0	--	2
0,	1,	1	--	3
1,	0,	0	--	5
1,	0,	1	--	7
1,	1,	0	--	9
1,	1,	1	--	15

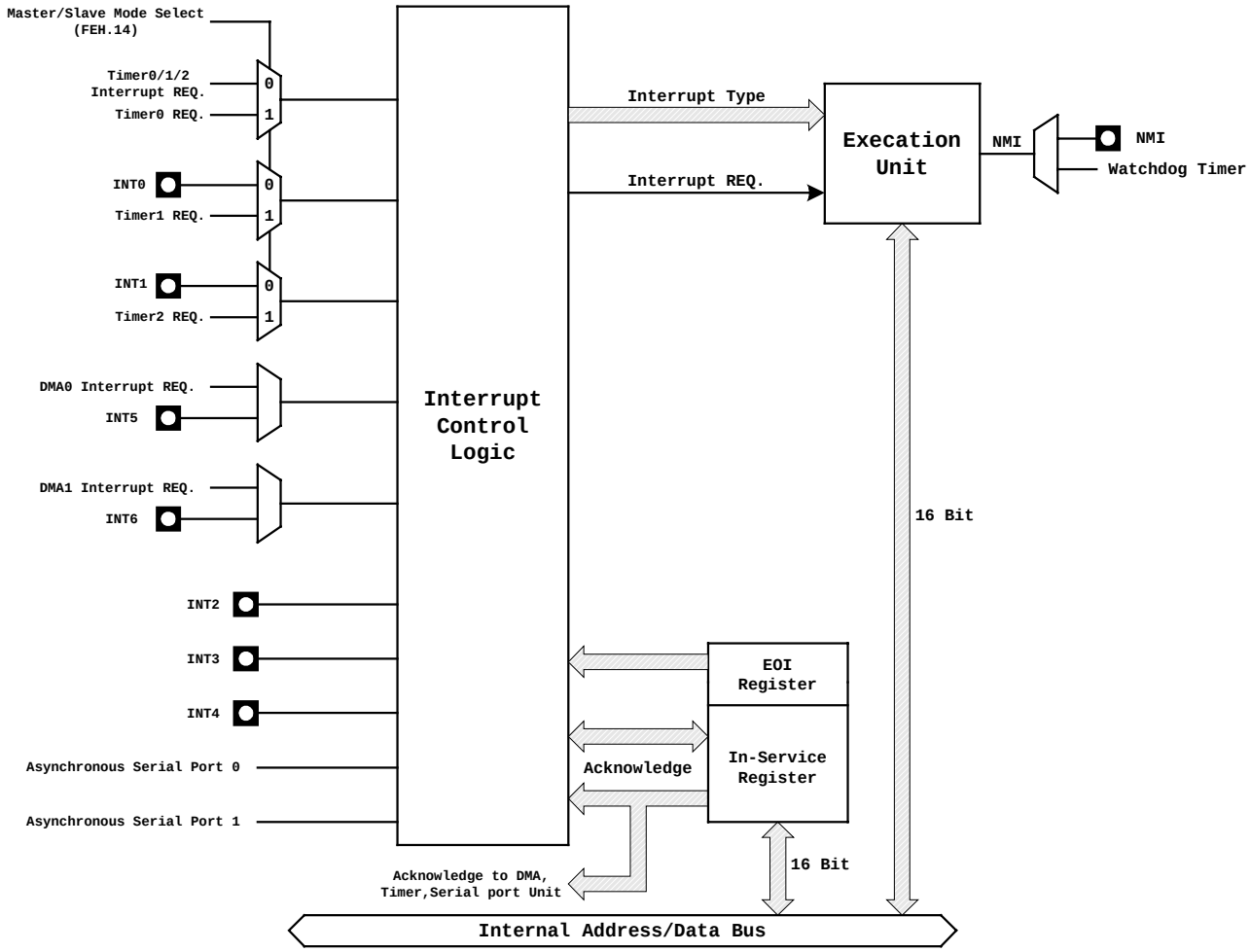
Bit 2: **R2**, Ready Mode. This bit is configured to enable/disable the wait states inserted for the $\overline{PCS3}$ - $\overline{PCS0}$ chip selects. The R3, R1 and R0 bits determine the number of wait state to be inserted.

Set 1: external ready is ignored

Set 0: external ready is required

14. Interrupt Controller Unit

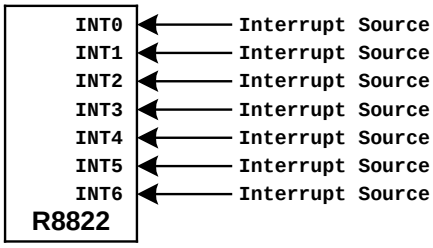
There are 16 interrupt requests source connected to the controller: 7 maskable interrupt pins (INT0 – INT6); 2 non-maskable interrupts (NMI pin and WDT) ; 7 internal unit request sources (Timer 0, 1 and 2 ;DMA 0 and 1; Asynchronous serial port 0 and 1).



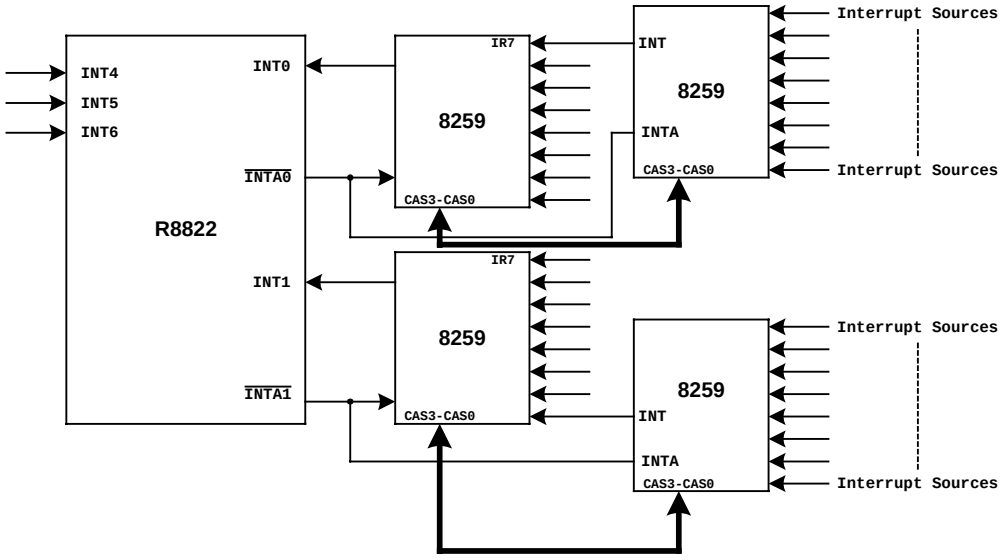
Interrupt Control Unit Block Diagram

14.1 Master Mode and Slave Mode

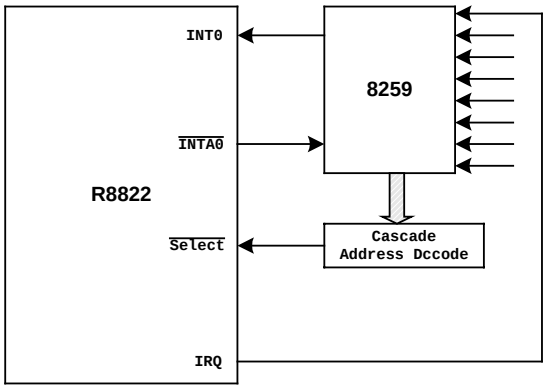
The interrupt controller can be programmed as a master or slave mode. (to program FEh [14]). The master mode has two connections: Fully Nested Mode connection or Cascade Mode connection.



Fully Nested Mode Connections



Cascade Mode Connection



Slave Mode Connection

14.2 Interrupt Vector, Type and Priority

The following table shows the interrupt vector addresses, type and the priority. The maskable interrupt priority can be changed by programming the priority registers. The Vector addresses for each interrupt are fixed.

Interrupt source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Opcode Exception	06h	18h		1	
ESC Opcode Exception	07h	1Ch		1	
Timer 0	08h	20h	08h	2-1	*/**
Reserved	09h				
DMA 0/INT5	0Ah	28h	0Ah	3	**
DMA 1/INT6	0Bh	2Ch	0Bh	4	**
INT0	0Ch	30h	0Ch	5	
INT1	0Dh	34h	0Dh	6	
INT2	0Eh	38h	0Eh	7	
INT3	0Fh	3Ch	0Fh	8	
INT4	10h	40h	10h	9	
Asynchronous Serial port 1	11h	44h	11h	9	
Timer 1	12h	48h	08h	2-2	*/**
Timer 2	13h	4Ch	08h	2-3	*/**
Asynchronous Serial port 0	14h	50h	14h	9	
Reserved	15h-1Fh				

Note * : When the interrupt occurs in the same time, the priority is (1-1 > 1-2) ; (2-1> 2-2 > 2-3)

Note **: The interrupt types of these sources are programmable in slave mode.

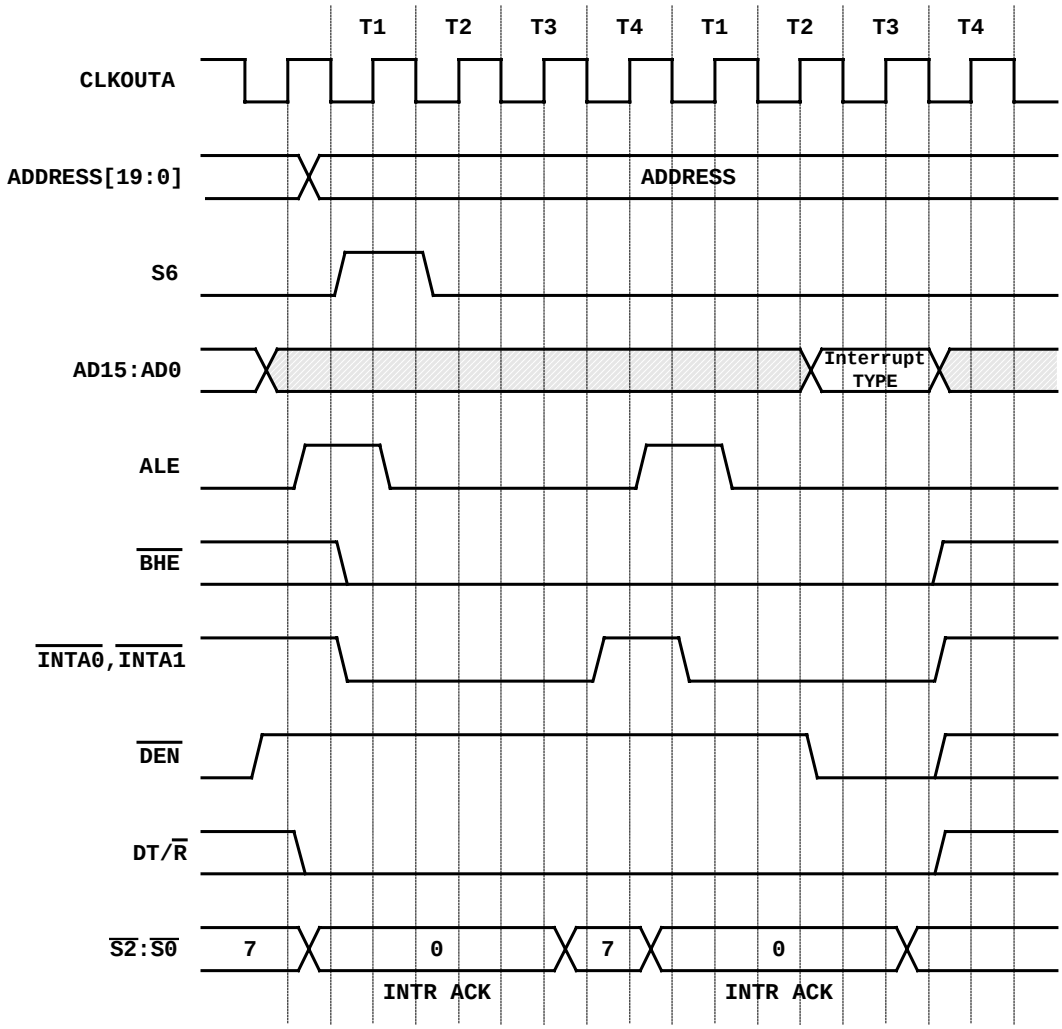
14.3 Interrupt Requests

When an interrupt is requested, the internal interrupt controller verifies the interrupt is enabled (the IF flag is enabled, no MSK bit set) and that there are no higher priority interrupt requests being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-triggered) to request the interrupt controller service, and the INT pins must be held till the microcontroller enters the interrupt service routine. There is no interrupt-acknowledged output when running in fully nested mode, so the PIO pins should be used to simulate the interrupt-acknowledged pin if necessary.

14.4 Interrupt Acknowledge

The processor requires the interrupt type as an index into the interrupt table. An internal or external controller can provide the interrupt type. The internal interrupt controller provides the interrupt type to processor without external bus cycles generation. When an external interrupt controller is providing the interrupt type, the processor generates two acknowledged bus cycles, and the interrupt type is written to the AD15-AD0 lines by the external interrupt controller.



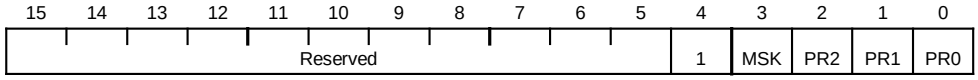
INTERRUPT ACKNOWLEDGE CYCLE (CASECADE OR SLAVE MODE)

14.5 Programming the Registers

Software is used to program the registers (**Master mode:** 44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h, 22h; **Slave Mode:** 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 22h, 20h) to define the interrupt controller operation.

Serial Port 0 Interrupt Control Register

Offset : 44h
Reset Value : 001Fh



(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of the asynchronous serial port 0.

Set 0: Enable the serial port 0 interrupt.

Bit 2-0: PR2-PR0, Priority. These bits determine the priority of the serial port related to the other interrupt signals.

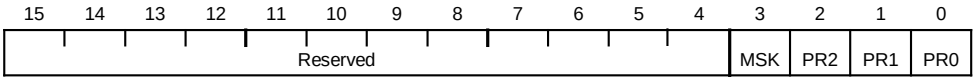
The priority selection:

PR2, **PR1**, **PR0** -- **Priority**

0 , 0 , 0 -- 0 (High)
0 , 0 , 1 -- 1
0 , 1 , 0 -- 2
0 , 1 , 1 -- 3
1 , 0 , 0 -- 4
1 , 0 , 1 -- 5
1 , 1 , 0 -- 6
1 , 1 , 1 -- 7 (Low)

Serial Port 1 Interrupt Control Register

Offset : 42h
Reset Value : 000Fh



(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of the asynchronous serial port 1.

Set 0: Enable the serial port 1 interrupt.

Bit 2-0: PR2-PR0, Priority. These bits determine the priority of the serial port related to the other interrupt signals.

The priority selection:

PR2, **PR1**, **PR0** -- **Priority**

0	,	0 ,	0	--	0 (High)
0	,	0 ,	1	--	1
0	,	1 ,	0	--	2
0	,	1 ,	1	--	3
1	,	0 ,	0	--	4
1	,	0 ,	1	--	5
1	,	1 ,	0	--	6
1	,	1 ,	1	--	7 (Low)

INT4 Control Register

Offset : 40h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-8, bit 6-5: Reserved

Bit 7: ETM, Edge trigger mode enable. When this bit is set to 1 and bit 4 set to 0, an interrupt is triggered by an edge, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of INT4

Set 0: Enable the INT4 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT3 Control Register

Offset : 3Eh
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15- 8, bit 6-5: Reserved

Bit 7: ETM, Edge trigger mode enable. When this bit is set to 1 and bit 4 set to 0, an interrupt is triggered by an edge, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of INT3

Set 0: Enable the INT3 interrupt.

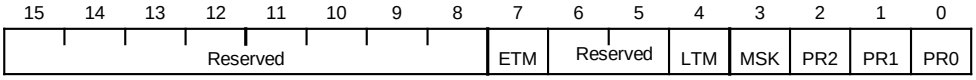
Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT2 Control Register

Offset : 3Ch

Reset Value : 000Fh



(Master Mode)

Bit 15-8, bit 6-5: Reserved

Bit 7: ETM, Edge trigger mode enable. When this bit is set to 1 and bit 4 set to 0, an interrupt is triggered by an edge, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of INT2

Set 0: Enable the INT2 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT1 Control Register **Offset : 3Ah**
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-8: Reserved

Bit 7: ETM, Edge trigger mode enable. When this bit is set to 1 and bit 4 set to 0, an interrupt is triggered by an edge, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 6: SFNM, Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT1

Bit 5: C, Cascade Mode. Set this bit to 1 to enable the cascade mode for INT1 or INT0.

Bit 4: LTM, Level-Triggered Mode.

Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of INT1

Set 0: Enable the INT1 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT1 Control Register **Offset : 3Ah**
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MSK	PR2	PR1	PR0

(Slave Mode), This register is for timer 2 interrupt control, reset value is 0000h

Bit 15- 4: Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of Timer 2

Set 0: Enable the Timer 2 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT0 Control Register **Offset : 38h**
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-8: Reserved

Bit 7: ETM, Edge trigger mode enable. When this bit is set to 1 and bit 4 set to 0, an interrupt is triggered by an edge, which goes from low to high. The low to high edge will be latched (one level) till this interrupt is serviced.

Bit 6: SFNM, Special Fully Nested Mode. Set 1: Enable the special fully nested mode of INT0.

Bit 5: C, Cascade Mode. Set this bit to 1 to enable the cascade mode for INT1 or INT0.

Bit 4: LTM, Level-Triggered Mode. Set 1: An interrupt is triggered by high active level.

Set 0: An interrupt is triggered by the low to high edge.

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of INT0

Set 0: Enable the INT0 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

INT0 Control Register

Offset : 38h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MSK	PR2	PR1	PR0

(Slave Mode), For Timer 1 interrupt control register, reset value is 0000h

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of timer 1

Set 0: Enable the timer 1 interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

DMA 1/INT6 Interrupt Control Register

Offset : 36h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the DMA 1 controller

Set 0: Enable the DMA 1 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

DMA 1/INT6 Interrupt Control Register

Offset : 36h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode), reset value is 0000h

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the DMA 1 controller

Set 0: Enable the DMA 1 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

DMA 0/INT5 Interrupt Control Register

Offset : 34h
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the DMA 0 controller

Set 0: Enable the DMA 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

DMA 0/INT5 Interrupt Control Register

Offset : 34h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask.

Set 1: Mask the interrupt source of the DMA 0 controller

Set 0: Enable the DMA 1 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

Timer Interrupt Control Register **Offset : 32h**
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the timer controller

Set 0: Enable the timer controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

Timer Interrupt Control Register **Offset : 32h**
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode)

Bit 15-4: Reserved

Bit 3: MSK, Mask. Set 1: Mask the interrupt source of the timer 0 controller

Set 0: Enable the timer 0 controller interrupt.

Bit 2-0: PR, Interrupt Priority

These bit settings for priority selection are the same as those of bit 2-0 of Register 44h.

Interrupt Status Register **Offset : 30h**
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved												TMR2	TMR1	TMR0

(Master Mode), Reset value undefined

Bit 15: DHLT, DMA Halt.

Set 1: Halt any DMA activity when non-maskable interrupts occurs.

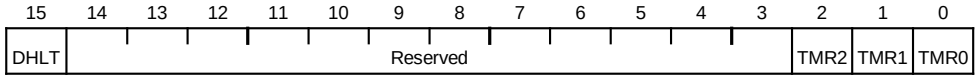
Set 0: When an IRET instruction is executed.

Bit 14-3: Reserved.

Bit 2-0: TMR2-TMR0,

Set 1: Indicates the corresponding timer has an interrupt request pending.

Interrupt Status Register **Offset : 30h**
Reset Value : 0000h



(Slave Mode)

Bit 15: DHLT, DMA Halt.

Set 1: Halt any DMA activity when non-maskable interrupts occur.

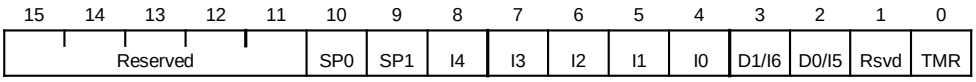
Set 0: When an IRET instruction is executed.

Bit 14-3: Reserved.

Bit 2-0: TMR2-TMR0,

Set 1: Indicates the corresponding timer has an interrupt request pending.

Interrupt Request Register **Offset : 2Eh**
Reset Value : —



(Master Mode)

The Interrupt Request register is a read-only register. For internal interrupts (SP0, SP1, D1/I6, D0/I5, and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT4-INT0 external interrupts, the corresponding bit (I4-I0) reflects the current value of the external signal.

Bit 15-11: Reserved.

Bit 10: SP0, Serial Port 0 Interrupt Request. Indicates the interrupt state of the serial port 0.

Bit 9: SP1, Serial Port 1 Interrupt Request. Indicates the interrupt state of the serial port 1.

Bit 8-4: I4-I0, Interrupt Requests.

Set 1: The corresponding INT pin has an interrupt pending.

Bit 3-2: D1/I6-D0/I5, DMA Channel or INT Interrupt Request.

Set 1: The corresponding DMA channel or INT has an interrupt pending.

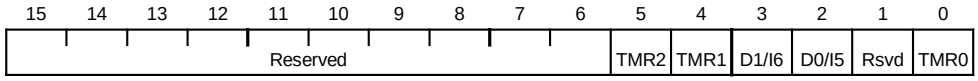
Bit 1: Reserved.

Bit 0: TMR, Timer Interrupt Request.

Set 1: The timer control unit has an interrupt pending.

Interrupt Request Register

Offset : 2Eh
Reset Value : 0000h



(Slave Mode)

The Interrupt Request register is a read-only register. For internal interrupts (D1/I6, D0/I5, TMR2, TMR1, and TMR0), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge.

Bit 15-6: Reserved.

Bit 5-4: TMR2/TMR1, Timer2/Timer1 Interrupt Request.

Set 1: Indicates the state of any interrupt requests form the associated timer.

Bit 3-2: D1/I6-D0/I5, DMA Channel or INT Interrupt Request.

Set 1: Indicates the corresponding DMA channel or INT has an interrupt pending.

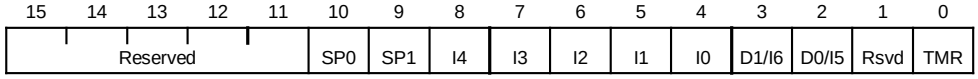
Bit 1: Reserved.

Bit 0: TMR0, Timer 0 Interrupt Request.

Set 1: Indicates the state of an interrupt request from Timer 0.

Interrupt In-Service Register

Offset : 2Ch
Reset Value : 0000h



(Master Mode)

The bits in the INSERV register are set by the interrupt controller when the interrupt is taken. Each bit in the register is cleared by writing the corresponding interrupt type to the EOI register.

Bit 15-11: Reserved.

Bit 10: SP0, Serial Port 0 Interrupt In-Service. Set 1: the serial port 0 interrupt is currently being serviced.

Bit 9: SP1, Serial Port 1 Interrupt In-Service. Set 1: the serial port 1 interrupt is currently being serviced.

Bit 8-4: I4-I0, Interrupt In-Service. Set 1: the corresponding INT interrupt is currently being serviced.

Bit 3-2: D1/I6-D0/I5, DMA Channel or INT Interrupt In-Service.

Set 1: the corresponding DMA channel or INT interrupt is currently being serviced.

Bit 1: Reserved.

Bit 0: TMR, Timer Interrupt In-Service. Set 1: the timer interrupt is currently being serviced.

Interrupt In-Service Register

Offset : 2Ch
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/I6	D0/I5	Rsvd	TMR0

(Slave Mode)

The bits in the In-Service register are set by the interrupt controller when the interrupt is taken. The in-service bits are cleared by writing to the EOI register.

Bit 15-6: Reserved.

Bit 5-4: TMR2-TMR1, Timer2/Timer1 Interrupt In-Service.

Set 1: the corresponding timer interrupt is currently being serviced.

Bit 3-2: D1/I6-D0/I5, DMA Channel or INT Interrupt In-Service.

Set 1: the corresponding DMA Channel or INT Interrupt is currently being serviced.

Bit 1: Reserved.

Bit 0: TMR0, Timer 0 Interrupt In-Service.

Set 1: the Timer 0 interrupt is currently being serviced.

Priority Mask Register

Offset : 2Ah
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Master Mode)

Determine the minimum priority level at which maskable interrupts can generate an interrupt.

Bit 15-3: Reserved.

Bit 2-0: PRM2-PRM0, Priority Field Mask. Determine the minimum priority that is required in order for a maskable interrupt source to generate an interrupt.

Priority	PR2-PR0
(High) 0	000
1	001
2	010
3	011
4	100
5	101
6	110
(Low) 7	111

Priority Mask Register **Offset : 2Ah**
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Slave Mode)

Determine the minimum priority level at which maskable interrupts can generate an interrupt.

Bit 15-3: Reserved.

Bit 2-0: PRM2-PRM0, Priority Field Mask. Determine the minimum priority that is required in order for a maskable interrupt source to generate an interrupt.

Priority	PR2-PR0
(High) 0	000
1	001
2	010
3	011
4	100
5	101
6	110
(Low) 7	111

Interrupt Mask Register **Offset : 28h**
Reset Value : 07FDh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	I4	I3	I2	I1	I0	D1/I6	D0/I5	Res	TMR

(Master Mode)

Bit 15-11: Reserved.

Bit 10: SP0, Serial Port 0 Interrupt Mask. The state of the mask bit of the asynchronous serial port 0 interrupt.

Bit 9: SP1, Serial Port 1 Interrupt Mask. The state of the mask bit of the asynchronous serial port 1 interrupt.

Bit 8-4: I4-I0, Interrupt Masks. Indicates the state of the mask bit of the corresponding interrupt.

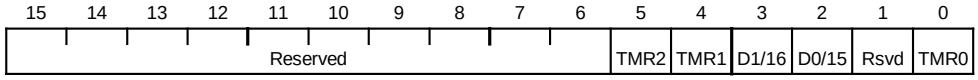
Bit 3-2: D1/I6-D0/I5, DMA Channel or INT Interrupt Masks.

Indicates the state of the mask bit of the corresponding DMA Channel or INT interrupt.

Bit 1: Reserved.

Bit 0: TMR, Timer Interrupt Mask. The state of the mask bit of the timer control unit.

Interrupt Mask Register **Offset : 28h**
Reset Value : 003Dh



(Slave Mode)

Bit 15-6: Reserved.

Bit 5-4: TMR2-TMR1, Timer 2/Timer1 Interrupt Mask. The state of the mask bit of the Timer Interrupt Control register.

Set 1: Timer2 or Time1 has its interrupt requests masked

Bit 3-2: D1/I6-D0/I5, DMA Channel or INT Interrupt Mask.

Indicates the state of the mask bits of the corresponding DMA or INT6/INT5 control register.

Bit 1: Reserved.

Bit 0: TMR0, Timer 0 Interrupt Mask. The state of the mask bit of the Timer Interrupt Control Register

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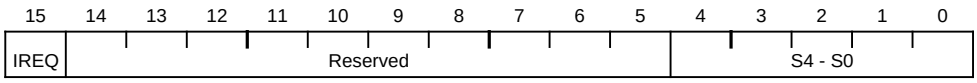
Poll Status Register **Offset : 26h**
Reset Value : —



(Master Mode)

The Poll Status (POLLST) register mirrors the current state of the Poll register. The POLLST register can be read without affecting the current interrupt request.

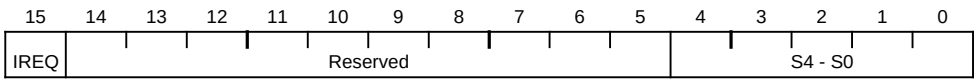
Bit 15: IREQ, Interrupt Request.

Set 1: if an interrupt is pending. The S4-S0 field contains valid data.

Bit 14-5: Reserved.

Bit 4-0: S4-S0, Poll Status. Indicate the interrupt type of the highest priority pending interrupt.

Poll Register **Offset : 24h**
Reset Value : —



(Master Mode)

When the Poll register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Poll register.

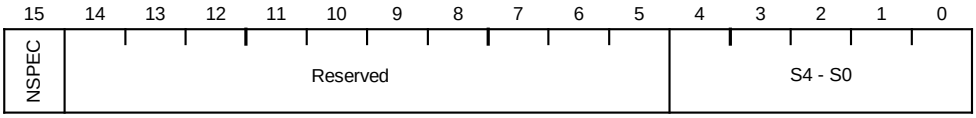
Bit 15: IREQ, Interrupt Request. Set 1: if an interrupt is pending. The S4-S0 field contains valid data.

Bit 14-5: Reserved.

Bit 4-0: S4-S0, Poll Status. Indicate the interrupt type of the highest priority pending interrupt.

End-of-Interrupt Register

Offset : 22h
Reset Value : —



(Master Mode)

Bit 15: NSPEC, Non-Specific EOI. Set 1: indicates non-specific EOI.

Set 0: indicates the specific EOI interrupt type in S4-S0.

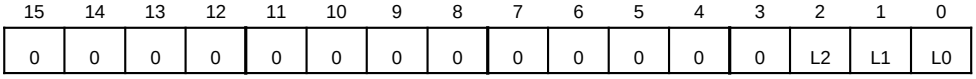
Bit 14-5: Reserved.

Bit 4-0: S4-S0, Source EOI Type. Specify the EOI type of the interrupt that is currently being processed.

Note: We suggest the specific EOI is the most secure method to use for resetting In-Service bit.

Specific End-of-Interrupt Register

Offset : 22h
Reset Value : 0000h



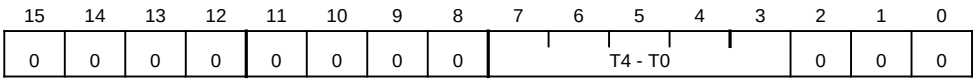
(Slave Mode)

Bit 15-3: Reserved.

Bit 2-0: L2-L0, Interrupt Type. Encoded value indicates the priority of the IS (interrupt service) bit to reset. Writes to these bits cause an EOI to be issued for the interrupt type in slave mode.

Interrupt Vector Register

Offset : 20h
Reset Value : —



(Slave Mode)

Bit 15-8: Reserved

Bit 7-3: T4-T0, Interrupt Type. The following interrupt type of slave mode can be programmed.

Timer 2 interrupt controller : (T4,T3,T2,T1,T0, 1, 0, 1)b

Timer 1 interrupt controller : (T4,T3,T2,T1,T0, 1, 0, 0)b

DMA 1 interrupt controller : (T4,T3,T2,T1,T0, 0, 1, 1)b

DMA 0 interrupt controller : (T4,T3,T2,T1,T0, 0, 1, 0)b

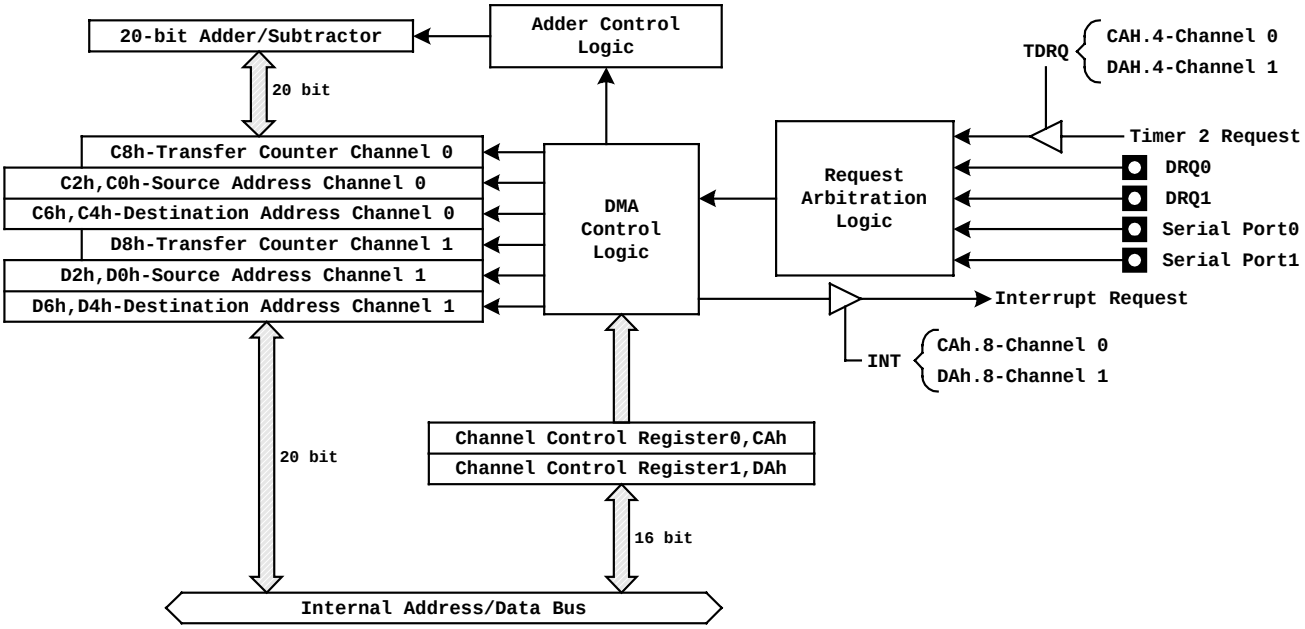
Timer 0 interrupt controller : (T4,T3,T2,T1,T0, 0, 0, 0)b

Bit 2-0: Reserved

---

15. DMA Unit

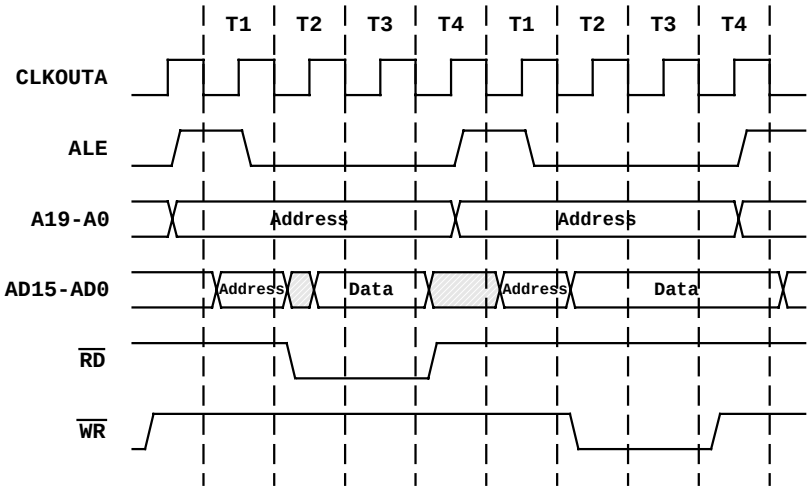
The DMA controller provides the data transfer between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA requests from one of three sources: external pins (DRQ0 for channel 0 or DRQ1 for channel 1), serial ports (port 0 or port 1) or Timer 2 overflow. The data transfer from source to destination can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (reads from sources and writes to destinations) for each data transfer.



DMA Unit Block

15.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfer) and the two bus cycles cannot be separated by a bus hold request, a refresh request or another DMA request. The registers (CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h and D0h) are used to configure and operate the two DMA channels.



Typical DMA Trarsfer

DMA0 Control Register

Offset : CAh (DMA0)
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/$\overline{IO}$	DDEC	DINC	SM/$\overline{IO}$	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	$\overline{B}$/W

Bit 15: DM/ $\overline{IO}$, Destination Address Space Select.

Set 1: The destination address is in memory space.

Set 0: The destination address is in I/O space.

Bit 14: DDEC, Destination Decrement.

Set 1: The destination address is automatically decremented after each transfer.

The $\overline{B}$ /W (bit 0) bit determines the decremented value which is by 1 or 2. When both of the DDEC and DINC bits are set to 1, the address remains constant.

Set 0: Disable the decrement function.

Bit 13: DINC, Destination Increment.

Set 1: The destination address is automatically incremented after each transfer.

The $\overline{B}$ /W (bit 0) bit determines the incremented value which is by 1 or 2.

Set 0: Disable the increment function.

Bit 12: SM/ $\overline{IO}$, Source Address Space Select.

Set 1: The Source address is in memory space.

Set 0: The Source address is in I/O space

Bit 11: SDEC, Source Decrement.

Set 1: The Source address is automatically decremented after each transfer.

The $\overline{B}$ /W (bit 0) bit determines the decremented value which is by 1 or 2. When both of the SDEC and SINC

bits are set to 1, the address remains constant.

Set 0: Disable the decrement function.

Bit 10: SINC, Source Increment.

Set 1: The Source address is automatically incremented after each transfer.

The $\overline{B}$/W (bit 0) bit determines the incremented value which is by 1 or 2

Set 0: Disable the increment function

Bit 9: TC, Terminal Count.

Set 1: The synchronized DMA transfer is terminated when the DMA transfer count register reaches 0.

Set 0: The synchronized DMA transfer is terminated when the DMA transfer count register reaches 0.

Unsynchronized DMA transfer is always terminated when the DMA transfer count register reaches 0, regardless the setting of this bit.

Bit 8: INT, Interrupt.

Set 1: DMA unit generates an interrupt request when the transfer count is complete.

The TC bit must be set to 1 to generate an interrupt.

Bit 7-6: SYN1-SYN0, Synchronization Type Selection.

SYN1 , **SYN0**	--	**Synchronization Type**
0 , 0	--	Unsynchronized
0 , 1	--	Source synchronized
1 , 0	--	Destination synchronized
1 , 1	--	Reserved

Bit 5: P, Priority.

Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred in the same time.

Bit 4: TDRQ, Timer Enable/Disable Request

Set 1: Enable the DMA requests from timer 2.

Set 0: Disable the DMA requests from timer 2.

Bit 3: EXT, External Interrupt Enable bit.

Set 1: The external pin is an interrupt pin. (DMA0 function is disabled.)

Set 0: The external pin is DRQ pin.

Bit 2: CHG, Changed Start Bit. This bit must be set to 1 when the ST bit is modified.

Bit 1: ST, Start/Stop DMA channel.

Set 1: Starts the DMA channel

Set 0: Stops the DMA channel

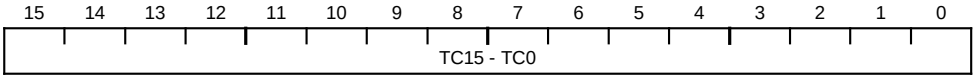
Bit 0: $\overline{B}$ /W, Byte/Word Select.

Set 1: The address is incremented or decremented by 2 after each transfer.

Set 0: The address is incremented or decremented by 1 after each transfer.

DMA0 Transfer Count Register

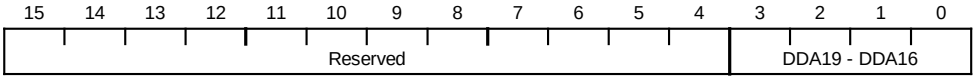
Offset : C8h (DMA0)
Reset Value : —



Bit 15-0: TC15-TC0, DMA 0 transfer Count. The value of this register is decremented by 1 after each transfer.

DMA0 Destination Address High Register

Offset : C6h (DMA0)
Reset Value : —

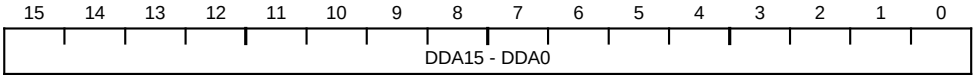


Bit 15-4: Reserved

Bit 3-0: DDA19-DDA16, High DMA 0 Destination Address. These bits are mapped to A19- A16 during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA0 Destination Address Low Register

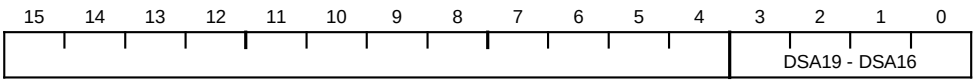
Offset : C4h (DMA0)
Reset Value : —



Bit 15-0: DDA15-DDA0, Low DMA 0 Destination Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DDA19-DDA0) will be incremented or decremented by 2 after each DMA transfer.

DMA0 Source Address High Register

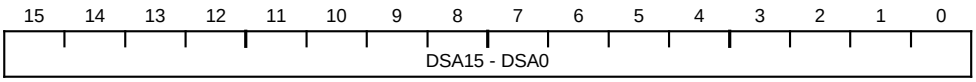
Offset : C2h (DMA0)
Reset Value : —



Bit 15-4: Reserved

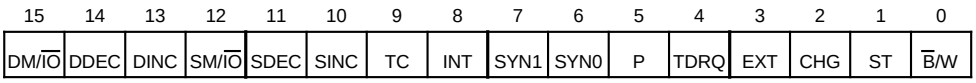
Bit 3-0: DSA19-DSA16, High DMA 0 Source Address. These bits are mapped to A19- A16 during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA0 Source Address Low Register **Offset : C0h (DMA0)**
Reset Value : ——



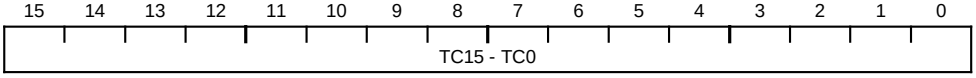
Bit 15-0: DSA15-DSA0, Low DMA 0 Source Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DSA19-DSA0) will be incremented or decremented by 2 after each DMA transfer.

DMA1 Control Register **Offset : DAh (DMA1)**
Reset Value : ----



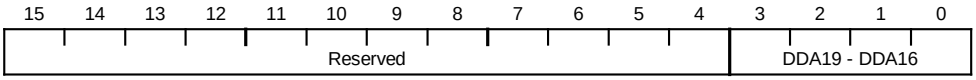
The definitions of Bit 15-0 for DMA1 are the same as those of Bit 15-0 of register CAh for DMA0.

DMA1 Transfer Count Register **Offset : D8h (DMA1)**
Reset Value : ——



Bit 15-0: TC15-TC0, DMA 1 transfer Count. The value of this register is decremented by 1 after each transfer.

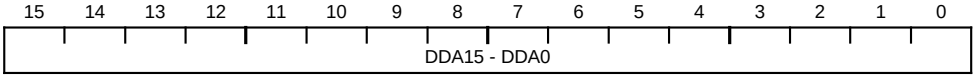
DMA1 Destination Address High Register **Offset : D6h (DMA1)**
Reset Value : ——



Bit 15-4: Reserved

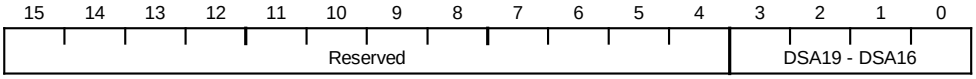
Bit 3-0: DDA19-DDA16, High DMA 1 Destination Address. These bits are mapped to A19- A16 during a DMA transfer when the destination address is in memory space or I/O space. If the destination address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA1 Destination Address Low Register Offset : D4h (DMA1)
Reset Value : —



Bit 15-0: DDA15-DDA0, Low DMA 1 Destination Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DDA19-DDA0) will be incremented or decremented by 2 after each DMA transfer.

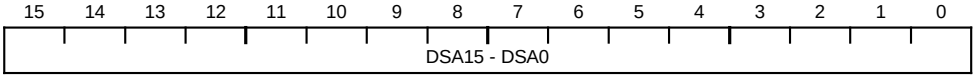
DMA1 Source Address High Register Offset : D2h (DMA1)
Reset Value : —



Bit 15-4: Reserved

Bit 3-0: DSA19-DSA16, High DMA 1 Source Address. These bits are mapped to A19- A16 during a DMA transfer when the source address is in memory space or I/O space. If the source address is in I/O space (64Kbytes), these bits must be programmed to 0000b.

DMA1 Source Address Low Register Offset : D0h (DMA1)
Reset Value : —

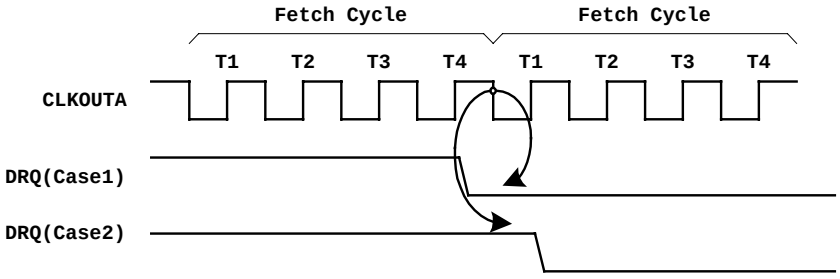


Bit 15-0: DSA15-DSA0, Low DMA 1 Source Address. These bits are mapped to A15- A0 during a DMA transfer. The value of (DSA19-DSA0) will be incremented or decremented by 2 after each DMA transfer.

15.2 External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of CLKOUTA. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. And no DMA acknowledge is provided, since the chip-selects ($\overline{\text{MCSx}}$ and $\overline{\text{PCSx}}$) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

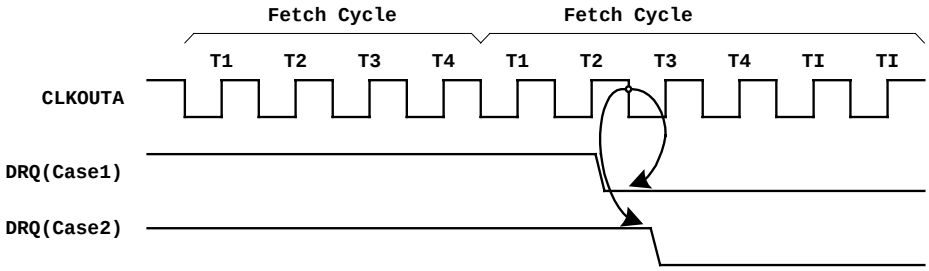
DMA transfer can be either source or destination synchronized, and it can also be unsynchronized. The Source-Synchronized Transfer figure shows the typical source-synchronized transfer which provides the source device at least three clock cycles from the time it is acknowledged to de-assert its DRQ line.



NOTES:
Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current source synchronized transfer will be immediately followed by antoher DMA transfer.

Source-Synchronized Transfers

The Destination-Synchronized Transfer figure shows the typical destination-synchronized transfer which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



NETES:
Case1 : Current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current destination synchronized transfer will be immediately followed by another DMA transfer.

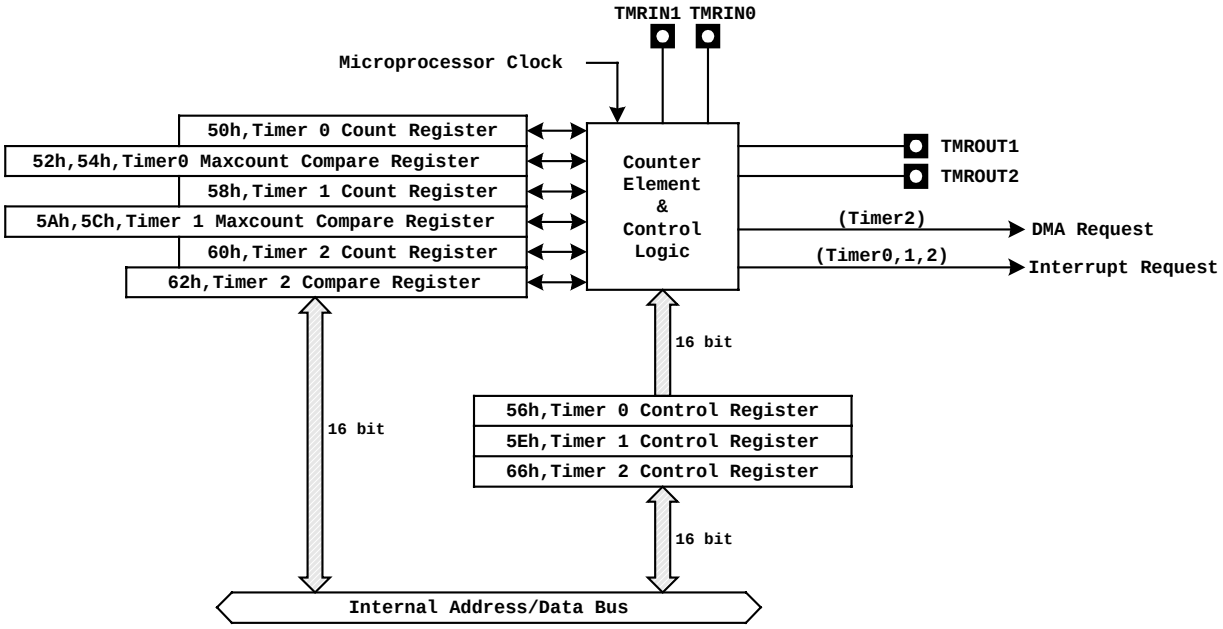
Destination-Synchronized Transfers

15.3 Serial Port/DMA Transfer

The serial port data can be DMA transfer to or from memory (or IO) space. And the $\overline{B}$/W bit of DMA control Register must be set to 1 for byte transfer. The map address of Transmit Data Register is written to the DMA Destination Address Register and the memory (or I/O) address is written to the DMA Source Address Register, when the data are transmitted. The map address of Receive Data Register is written to the DMA Source Address Register and the memory (or I/O) address is written to the DMA Destination Address Register, when the data are received.

Software is used to program the Serial Port Control Register to perform the serial port/ DMA transfer. When a DMA channel is in use by a serial port, the corresponding external DMA request signal is deactivated. For DMA to the serial port, the DMA channel should be configured as being destination-synchronized. For DMA from the serial port, the DMA channel should be configured as being source-synchronized.

16. Timer Control Unit



Timer / Counter Unit Block

There are three 16-bit programmable timers in the R8822. The timer operation is independent of the CPU. The three timers can be programmed as a timer element or as a counter element. Timers 0 and 1 are each connected to two external pins (TMRIN0, TMROUT0, TMRIN1 and TMROUT1) which can be used to count or time external events, or used to generate variable-duty-cycle waveforms. Timer 2 is not connected to any external pins. It can be used as a pre-scaler to timer 0 and timer 1 or as a DMA request source.

Timer 0 Mode / Control Register

Offset : 56h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit 15: EN, Enable Bit.

Set 1: The timer 0 is enabled.

Set 0: The timer 0 is inhibited from counting.

The $\overline{INH}$ bit must be set to 1 when the EN bit is written, and the $\overline{INH}$ and EN bits must be in the same write.

Bit 14: $\overline{INH}$, Inhibit Bit. This bit allows selective updating the EN bit. The $\overline{INH}$ bit must be set to 1 when the EN is written, and both the $\overline{INH}$ and EN bits must be in the same write. This bit is not stored and always read as 0.

Bit 13: INT, Interrupt Bit.

Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in

dual max-count mode, an interrupt is generated each time the count reaches max-count A or max-count B

Set 0: Timer 0 will not issue interrupt requests.

Bit 12: RIU, Register in Use Bit.

Set 1: The Maxcount Compare B register of timer 0 is being used

Set 0: The Maxcount Compare A register of timer 0 is being used

Bit 11-6: Reserved.

Bit 5: MC, Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set each time either Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the INT bit (56h.13).

Bit 4: RTG, Re-trigger Bit. This bit defines the control function by the input signal of TMRIN0 pin. When EXT=1 (56h.2), this bit is ignored.

Set 1: Timer0 Count Register (50h) counts internal events; Reset the counting on every TMRIN0 input signal from low to high (rising edge trigger).

Set 0: Low input holds the timer 0 Count Register (50h) value; High input enables the counting which counts internal events.

The definition of setting the (EXT, RTG)

(0, 0) – Timer0 counts the internal events if the TMRIN0 pin remains high.

(0, 1) – Timer0 counts the internal events; count register reset on every rising transition on the TMRIN0 pin

(1, x) – TMRIN0 pin input acts as clock source and timer0 count register is incremented by one every external clock.

Bit 3: P, Pre-scaler Bit. This bit and EXT bit (56h.2) define the timer0 clock source.

The definition of setting the (EXT, P)

(0, 0) – Timer0 Count Register is incremented by one every four internal processor clock.

(0, 1) – Timer0 count register is incremented by one which is pre-scaled by timer 2.

(1, x) – TMRIN0 pin input acts as clock source and Timer0 Count Register is incremented by one every external clock.

Bit 2: EXT, External Clock Bit. Set 1: Timer0 clock source from external

Set 0: Timer0 clock source from internal

Bit 1: ALT, Alternate Compare Bit. This bit controls whether the timer runs in single or dual maximum count mode.

Set 1: Specify dual maximum count mode. In this mode, the timer counts to Maxcount Compare A and resets the count register to 0. Then the timer counts to Maxcount Compare B, resets the count register to 0 again, and starts over with Maxcount Compare A.

Set 0: Specify single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and reset to 0. Then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.

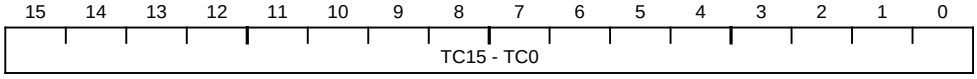
Bit 0: CONT, Continuous Mode Bit.

Set 1: The timer runs continuously.

Set 0: The timer will halt after each counting to the maximum count and the EN bit will be cleared.

Timer 0 Count Register

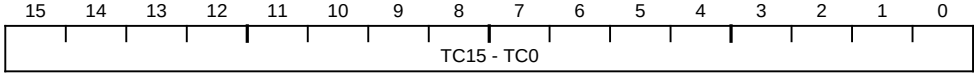
Offset : 50h
Reset Value : ——



Bit 15 – 0: TC15-TC0, Timer 0 Count Value. This register contains the current count of timer 0. The count is incremented by one every four internal processor clocks, or pre-scaled by timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN0 signal.

Timer 0 Maxcount Compare A Register

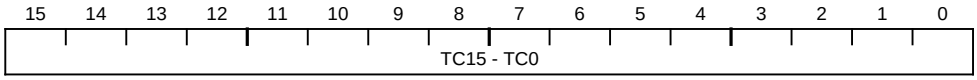
Offset : 52h
Reset Value : ——



Bit 15-0: TC15 – TC0, Timer 0 Compare A Value.

Timer 0 Maxcount Compare B Register

Offset : 54h
Reset Value : ——



Bit 15-0: TC15 – TC0, Timer 0 Compare B Value.

Timer 1 Mode / Control Register

Offset : 5Eh
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

These bit definitions for timer1 are the same as those of register 56h for timer 0.

Timer 1 Count Register

Offset : 58h
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15 – 0: TC15-TC0, Timer 1 Count Value. This register contains the current count of timer 1. The count is incremented by one every four internal processor clocks, or pre-scaled by timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN1 signal.

Timer 1 Maxcount Compare A Register

Offset : 5Ah
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

3Bit 15-0: TC15 – TC0, Timer 1 Compare A Value.

Timer 1 Maxcount Compare B Register

Offset : 5Ch
Reset Value : —

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC15 - TC0															

Bit 15-0: TC15 – TC0, Timer 1 Compare B Value.

Timer 2 Mode / Control Register

Offset : 66h
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	$\overline{INH}$	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit 15: EN, Enable Bit.

Set 1: Timer 2 is enabled.

Set 0: Timer 2 is inhibited from counting.

The $\overline{INH}$ bit must be set to 1 during the EN bit is written, and the $\overline{INH}$ and EN bits must be in the same write.

Bit 14: $\overline{INH}$, Inhibit Bit. This bit allows selective updating the EN bit. The $\overline{INH}$ bit must be set to 1 when the EN bit is written, and both the $\overline{INH}$ and EN bits must be in the same write. This bit is not stored and always read as 0.

Bit 13: INT, Interrupt Bit.

Set 1: An interrupt request is generated when the count register equals a maximum count.

Set 0: Timer 2 will not issue interrupt request.

Bit 12-6: Reserved.

Bit 5: MC, Maximum Count Bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the INT bit (66h.13).

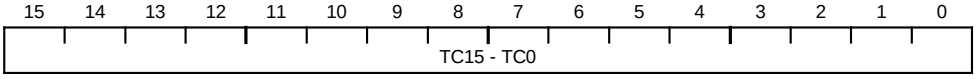
Bit 4-1: Reserved.

Bit 0: COUNT, Continuous Mode Bit.

Set 1: Timer is continuously running when it reaches the maximum count.

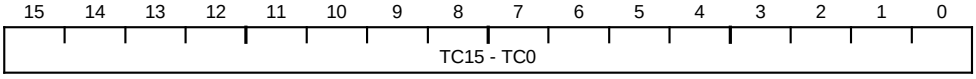
Set 0: The EN bit (66h.15) is cleared and the timer is held after each timer count reaches the maximum count.

Timer 2 Count Register — **Offset : 60h** — **Reset Value : —**



Bit 15 – 0: TC15-TC0, Timer 2 Count Value. This register contains the current count of timer 2. The count is incremented by one every four internal processor clocks.

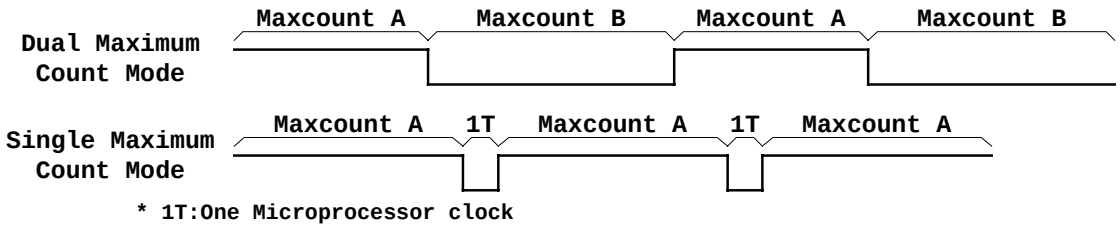
Timer 2 Maxcount Compare A Register — **Offset : 62h** — **Reset Value : —**



Bit 15-0: TC15 – TC0, Timer 2 Compare A Value.

16.1 Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count values. Timer 2 can use only one maximum count value. Timer 0 and timer1 can be configured to be a single or dual Maximum Compare count mode, the TMROUT0 or TMROUT1 signals can be used to generate waveforms of various duty cycles.



Timer/Counter Unit Output Modes

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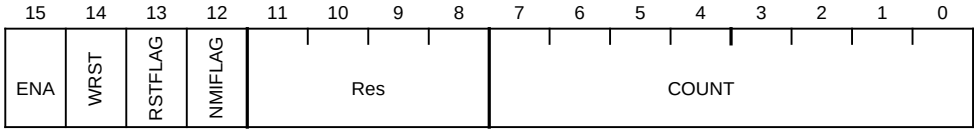
17. Watchdog Timer

R8822 has one independent watchdog timer, which is programmable. **The watchdog timer is active after reset** and the timeout count is with a maximum count value. The keyed sequence (3333h, CCCCh) must be written to the register (E6h) first, then the new configuration to the Watchdog Timer Control Register. It is a single write, so every writing to Watchdog Timer Control Register must follow this rule.

When the watchdog timer activates, an internal counter is counting. If this internal count is over the watchdog timer duration, the watchdog timeout happens. The keyed sequence (AAAAh, 5555h) must be written to the register (E6h) to reset the internal count and prevent the watchdog timeout. The internal count should be reset before the Watchdog Timer timeout period is modified to ensure that an immediate timeout will not occur.

Watchdog Timer Control Register **Offset : E6h**

Reset Value : C080h



Bit 15: ENA, Enable Watchdog Timer.

Set 1: Enable Watchdog Timer.

Set 0: Disable Watchdog Timer.

Bit 14: WRST, Watchdog Reset.

Set 1: WDT generates a system reset when WDT timeout count is reached.

Set 0: WDT generates an NMI interrupt when WDT timeout count is reached if the NMIFLAG bit is 0. If the NMIFLAG bit is 1, the WDT will generate a system reset when timeout.

Bit 13: RSTFLAG, Reset Flag. When watchdog timer reset event occurs, this bit will be set to 1 by hardware. This bit will be cleared by any keyed sequence write to this register or external reset. This bit is 0 after an external reset or 1 after a watchdog timer reset.

Bit 12: NMIFLAG, NMI Flag. After WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequence write to this register.

Bit 11-8: Reserved.

Bit 7-0: COUNT, Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.

a. The duration equation: **Duration** = 2^{Exponent} / **Frequency**

b. The Exponent of the COUNT setting:

(Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, Bit 0) = (Exponent)

(0 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (N/A)

(x , x , x , x, x , x , x , x) = (10)

(x , x , x , x, x , x , 1 , 0) = (20)

(x , x , x , x, x , 1 , 0 , 0) = (21)

(x , x , x , x, 1 , 0 , 0 , 0) = (22)

(x , x , x , 1, 0 , 0 , 0 , 0) = (23)

(x , x , 1 , 0, 0 , 0 , 0 , 0) = (24)

(x , 1 , 0 , 0, 0 , 0 , 0 , 0) = (25)

(1 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (26)

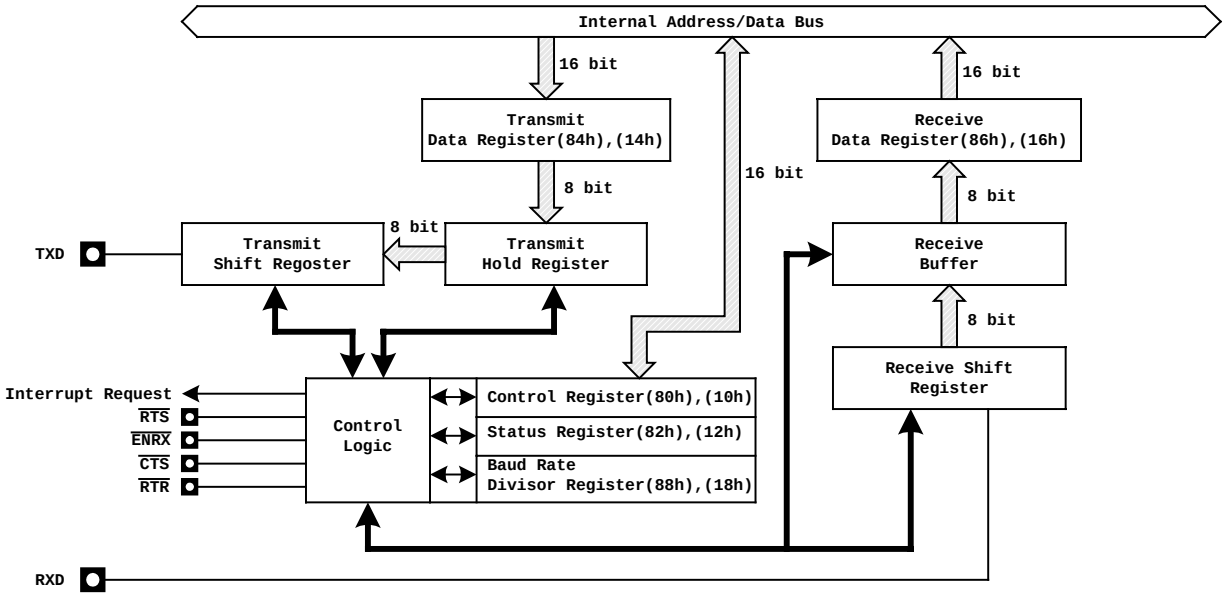
c. Watchdog timer Duration reference table:

Frequency\Exponent	10	20	21	22	23	24	25	26
20 MHz	51 us	52 ms	104 ms	209 ms	419 ms	838 ms	1.67 s	3.35 s
25 MHz	40 us	41 ms	83 ms	167 ms	335 ms	671 ms	1.34 s	2.68 s
33 MHz	30 us	31 ms	62 ms	125 ms	251 ms	503 ms	1.00 s	2.01 s
40 MHz	25 us	26 ms	52 ms	104 ms	209 ms	419 ms	838 ms	1.67 s

18. Asynchronous Serial Ports

R8822 has two asynchronous serial ports, which provide the TXD and RXD pins for the fully duplexed bi-directional data transfer and with handshaking signals $\overline{CTS}$, $\overline{ENRX}$, $\overline{RTS}$ and $\overline{RTR}$. The serial ports support: 9-bit, 8-bit or 7-bit data transfer; odd parity, even parity, or no parity; 1 stop bit; Error detection; DMA transfers through the serial port; Multi-drop protocol (9-bit) support; Double buffers for transmit and receive.

The receive/transmit clock is based on the microprocessor clock. The serial port can be used in power-saved mode, but the transfer rate must be adjusted to correctly reflect the new internal operating frequency. Software is used to program the registers (80h, 82h, 84h, 86h and 88h – for port 0; 10h, 12h, 14h, 16h and18h – for port 1) to configure the asynchronous serial ports.



Serial Port Block Diagram

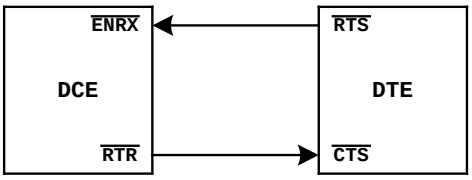
18.1 Serial Port Flow Control

The two serial ports are provided with two data pins (RXD and TXD) and two flow control signals ($\overline{RTS}$ and $\overline{RTR}$). Hardware flow control is enabled when the FC bit in the Serial Port control Register is set. And the flow control signals are configured by software to support several different protocols.

18.1.1 DCE/DTE Protocol

The R8822 can be as a DCE (Data Communication Equipment) or as a DTE (Data Terminal Equipment). This protocol provides flow control where one serial port is receiving data and the other serial port is sending data. To implement the DCE device, the ENRX bit should be set and the RTS bit should be cleared for the associated serial ports. To implement the DTE device, the ENRX bit should be cleared and the RTS bit should be set for the associated serial ports. The ENRX and RTS bits are in the register F2h.

The DCE/DTE protocol is asymmetric interface since the DTE device cannot signal the DCE device that is ready to receive data, and the DCE cannot send the request to send signals.



$\overline{RTS}$:Request to send
$\overline{CTS}$:Clear to send
$\overline{RTR}$:Ready to receive
$\overline{ENRX}$:Enable receiver request

DCE/DTE Protocol Connection

The DCE/DTE protocol communication steps:

a. DTE sends data to DCE

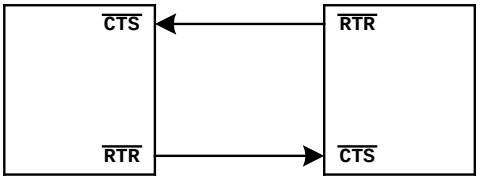
b. $\overline{RTS}$ signal is asserted by DTE when data is available.

c. The $\overline{RTS}$ signal is interpreted by the DCE device as a request to enable its receiver.

d. The DCE asserts the $\overline{RTR}$ signal to response that DCE is ready to receive data.

18.1.2 CTS/RTR Protocol

The serial port can be programmed as a CTS/RTS protocol by clearing both ENRX and RTS bits. This protocol is a symmetric interface, which provides flow control when both ports are sending and receiving data.



$\overline{CTS}$:Clear to send
$\overline{RTR}$:Ready to receive

CTS/RTR Protocol Connection

18.2 DMA Transfer to/from a Serial Port Function

DMA transfers to the serial port function are regarded as destination-synchronized DMA transfers. A new transfer is requested when the Transmit Holding Register is empty. When the port is configured for DMA transmits, the corresponding transmit interrupt is disabled regardless of the TXIE bit setting.

DMA transfers from the serial port function are regarded as source-synchronized DMA transfers. A new transfer is requested when the Receive Buffer contains valid data. When the port is configured for DMA receives, the corresponding receive interrupt is disabled regardless of the RXIE bit setting.

The DMA request is generated internally when a DMA channel is being used for serial port transfers. And the DRQ0 or DRQ1 is not active when a serial port DMA transfers. Hardware handshaking may be used in conjunction with serial port DMA transfers.

18.3 The Asynchronous Mode Description

There are 4 modes operating in the asynchronous serial port.

Mode1: Mode 1 is the 8-bit asynchronous communications mode. Each frame consists of a start bit, eight data bits and a stop bit. When parity is used, the eighth data bit becomes the parity bit.

Mode 2: Mode 2 is used together with Mode 3 for multiprocessor communications over a common serial link. In mode 2, the RX machine will not complete a reception unless the ninth data bit is a one. Any character received with the ninth bit equal to zero is ignored. No flags are set, no interrupts occur and no data is transferred to Receive Data Register. In mode 3, characters are received regardless of the state of the ninth data bit.

Mode 3: Mode 3 is the 9-bit asynchronous communications mode. Mode 3 is the same as mode 1 except that a frame contains nine data bits. The ninth data bit becomes the parity bit when the parity feature is enabled.

Mode 4: Mode 4 is the 7-bit asynchronous communications mode. Each frame consists of a start bit, seven data bits and a stop bit. Parity bit is not available in mode 4.

Serial Port 0 Control Register **Offset : 80h**

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA			RISE	BRK	TB8	FC	TXIE	RXIE	TMODE	RMODD	EVN	PE	MODE		

Bit 15-13: DMA, DMA Control Field. These bits configure the serial ports in use with DMA transfers.

DMA control bits

(Bit 15, bit 14, bit 13)b	---	**Receive**	---	**Transmit**
(0, 0, 0)	---	No DMA	---	No DMA
(0, 0, 1)	---	DMA 0	---	DMA 1

(0, 1, 0)	---	DMA 1	---	DMA 0
(0, 1, 1)	---	N/A	---	N/A
(1, 0, 0)	---	DMA 0	---	No DMA
(1, 0, 1)	---	DMA 1	---	No DMA
(1, 1, 0)	---	No DMA	---	DMA 0
(1, 1, 1)	---	No DMA	---	DMA 1

Bit 12: RSIE, Receive Status Interrupt Enable. An exception occurring during data reception or error detection will generate an interrupt.

Set 1: Enable the serial port 0 to generate an interrupt request.

Bit 11: BRK, Send Break.

Set this bit to 1, the TXD pin is always driven low.

Long Break: The TXD is driven low for greater than (2M+3) bit times;

Short break: The TXD is driven low for greater than M bit times;

* M= start bit + data bits number + parity bit + stop bit

Bit 10: TB8, Transmit Bit 8. This bit is transmitted as ninth data bit in mode 2 and mode 3. This bit is cleared after every transmission.

Bit 9: FC, Flow Control Enable.

Set 1: Enable the hardware flow control for serial port 0.

Set 0: Disable the hardware flow control for serial port 0.

Bit 8: TXIE, Transmitter Ready Interrupt Enable. When the Transmit Holding Register is empty (the THRE bit in Status Register is set), an interrupt will occur.

Set 1: Enable the Interrupt.

Set 0: Disable the interrupt.

Bit 7: RXIE, Receive Data Ready Interrupt Enable. When the receiver buffer contains valid data (the RDR bit in Status Register is set), it will generate an interrupt.

Set 1: Enable the Interrupt.

Set 0: Disable the interrupt.

Bit 6: TMODE, Transmit Mode.

Set 1: Enable the TX machines.

Set 0: Disable the TX machines.

Bit 5: RMODE, Receive Mode.

Set 1: Enable the RX machines.

Set 0: Disable the RX machines.

Bit 4: EVN, Even Parity. This bit is valid only when the PE bit is set.

Set 1: the even parity checking is enforced (even number of 1s in frame).

Set 0: odd parity checking is enforced (odd number of 1s in frame).

Bit 3: PE, Parity Enable.

Set 1: Enable the parity checking.

Set 0: Disable the parity checking.

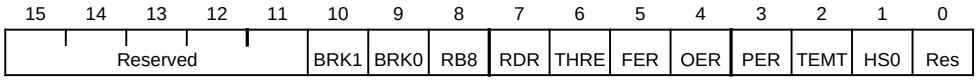
Bit 2-0: MODE, Mode of Operation.

(bit 2, bit 1, bit 0)	MODE	Data Bits	Parity Bits	Stop Bits
(0 , 0 , 1)	Mode 1	7 or 8	1 or 0	1
(0 , 1 , 0)	Mode 2	9	N/A	1
(0 , 1 , 1)	Mode 3	8 or 9	1 or 0	1
(1 , 0 , 0)	Mode 4	7	N/A	1

Serial Port 0 Status Register

Offset : 82h

Reset Value : —



The Serial Port 0 Status Register provides information about the current status of the serial port 0.

Bit 15-11: Reserved.

Bit 10: BRK1, Long Break Detected. This bit should be reset by software.

When a long break is detected, this bit will be set high.

Bit 9: BRK0, Short Break Detected. This bit should be reset by software.

When a short break is detected, this bit will be set high

Bit 8: RB8, Received Bit 8. This bit should be reset by software.

This bit contains the ninth data bit received in mode 2 and mode 3.

Bit 7: RDR, Received Data Ready. Read only.

The Received Data Register contains valid data. This bit is set high and can only be reset by reading the Serial Port 0 Receive Register.

Bit 6: THRE, Transmit Hold Register Empty. Read only.

When the Transmit Hold Register is ready to accept data, this bit will be set. This bit will be reset when data is written to the Transmit Hold Register.

Bit 5: FER, Framing Error detected. This bit should be reset by software.

This bit is set when a framing error is detected.

Bit 4: OER, Overrun Error Detected. This bit should be reset by software.

This bit is set when an overrun error is detected.

Bit 3: PER, Parity Error Detected. This bit should be reset by software.

This bit is set when a parity error (for mode 1 and mode 3) is detected.

Bit 2: TEMT, Transmitter Empty. This bit is read only.

When the Transmit Shift Register is empty, this bit will be set.

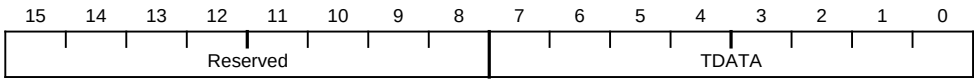
Bit 1: HS0, Handshake Signal 0. This bit is read only.

This bit reflects the inverted value of the external $\overline{CTS0}$ pin.

Bit 0: Reserved.

Serial Port 0 Transmit Register

Offset : 84h
Reset Value : —

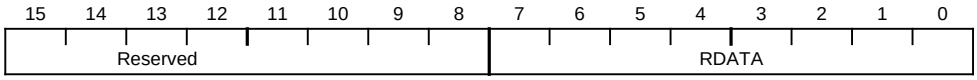


Bit 15-8: Reserved

Bit 7-0: TDATA, Transmit Data. This register is written by software with data to be transmitted on the serial port 0.

Serial Port 0 Receive Register

Offset : 86h
Reset Value : —

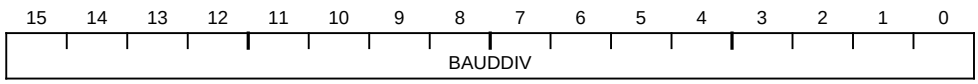


Bit 15-8: Reserved

Bit 7-0: RDATA, Received DATA. The RDR bit should be read as 1 before the RDATA register is read to avoid reading invalid data.

Serial Port 0 Baud Rate Divisor Register

Offset : 88h
Reset Value : 0000h



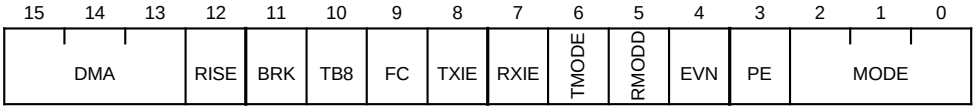
Bit 15-0: BAUDDIV, Baud Rate Divisor.

The general formula for baud rate divisor is **Baud Rate = Microprocessor Clock / (16 x BAUDDIV)**

For example, when the Microprocessor clock is 22.1184MHz and the BAUDDIV=12 (Decimal), the baud rate of serial port is 115.2k.

Serial Port 1 Control Register

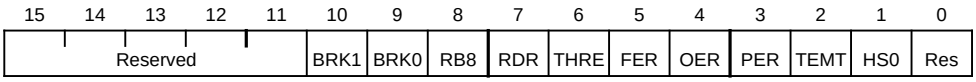
Offset : 10h
Reset Value : 0000h



These bit definitions are the same as those of Register 80h

Serial Port 1 Status Register

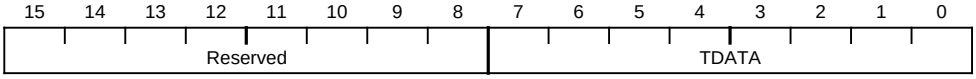
Offset : 12h
Reset Value : —



These bit definitions are the same as those of Register 82h

Serial Port 1 Transmit Register

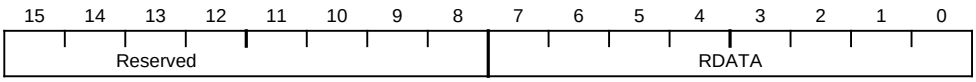
Offset : 14h
Reset Value : —



These bit definitions are the same as those of Register 84h

Serial Port 1 Receive Register

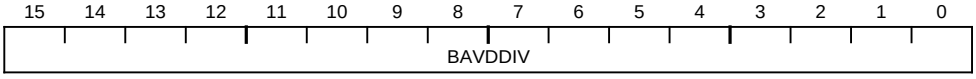
Offset : 16h
Reset Value : —



These bit definitions are the same as those of Register 86h

Serial Port 1 Baud Rate Divisor Register

Offset : 18h
Reset Value : 0000h



These bit definitions are the same as those of Register 88h.

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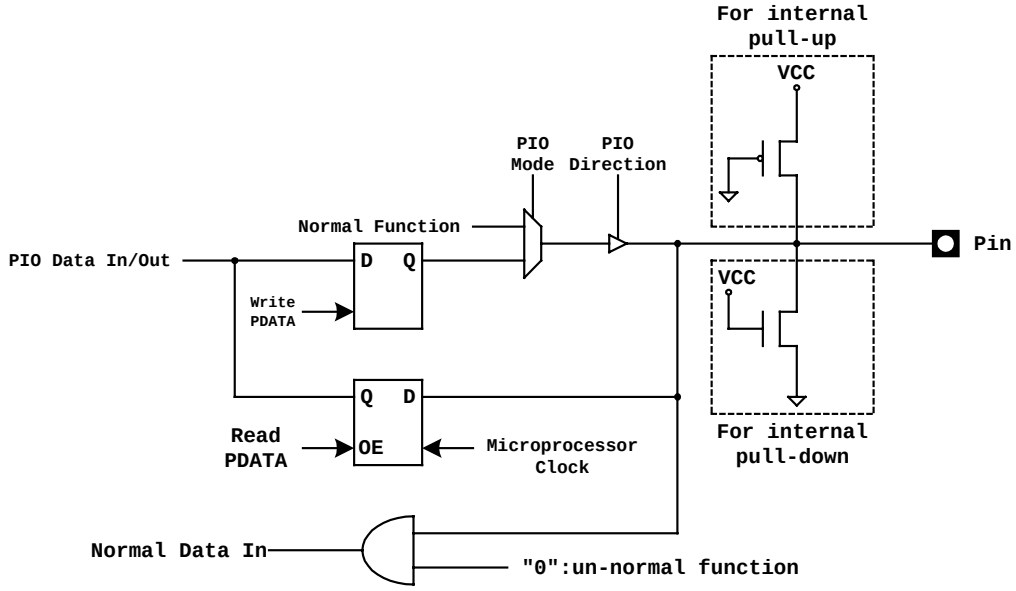
19. PIO Unit

R8822 provides 32 programmable I/O signals, which are multi-functional pins, with other normal function signals. Software is used to program the registers (7Ah, 78h, 76h, 74h, 72h and 70h) to configure these multi-functional pins for PIO or normal function.



PIO pin Operation Diagram

19.1 PIO Multi-Function Pin List Table

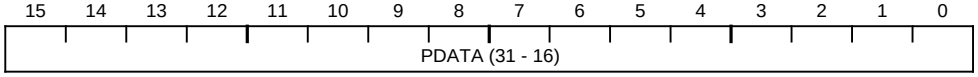
PIO No.	Pin No.(PQFP)	Multi Function	Reset status/PIO internal resistor
0	72	TMRIN1	Input with 10k pull-up
1	73	TMROUT1	Input with 10k pull-down
2	59	$\overline{\text{PCS6}}$ /A2	Input with 10k pull-up
3	60	$\overline{\text{PCS5}}$ /A1	Input with 10k pull-up
4	48	DT/ $\overline{\text{R}}$	Normal operation/ Input with 10k pull-up
5	49	$\overline{\text{DEN}}$	Normal operation/ Input with 10k pull-up
6	46	SRDY	Normal operation/ Input with 10k pull-down
7	22	A17/MA8	Normal operation/ Input with 10k pull-up
8	20	A18	Normal operation/ Input with 10k pull-up
9	19	A19	Normal operation/ Input with 10k pull-up
10	74	TMROUT0	Input with 10k pull-down
11	75	TMRIN0	Input with 10k pull-up
12	77	DRQ0/INT5	Input with 10k pull-up
13	76	DRQ1/INT6	Input with 10k pull-up
14	50	$\overline{\text{MCS0}}$	Input with 10k pull-up
15	51	$\overline{\text{MCS1}}$ / $\overline{\text{UCAS}}$	Input with 10k pull-up
16	66	$\overline{\text{PCS0}}$	Input with 10k pull-up

17	65	$\overline{PCS1}$	Input with 10k pull-up
18	63	$\overline{PCS2}$ / $\overline{CTS1}$ / $\overline{ENRX1}$	Input with 10k pull-up
19	62	$\overline{PCS3}$ / $\overline{RTS1}$ / $\overline{RTR1}$	Input with 10k pull-up
20	3	$\overline{RTS0}$ / $\overline{RTR0}$	Input with 10k pull-up
21	100	$\overline{CTS0}$ / $\overline{ENRX0}$	Input with 10k pull-up
22	2	TXD0	Input with 10k pull-down
23	1	RXD0	Input with 10k pull-down
24	68	$\overline{MCS2}$ / $\overline{LCAS}$	Input with 10k pull-up
25	69	$\overline{MCS3}$ / $\overline{RAS1}$	Input with 10k pull-up
26	97	$\overline{UZI}$	Input with 10k pull-up
27	98	TXD1	Input with 10k pull-up
28	99	RXD1	Input with 10k pull-up
29	96	S6/ $\overline{CLKDIV2}$	Input with 10k pull-up
30	52	INT4	Input with 10k pull-up
31	54	INT2	Input with 10k pull-up

PIO Data 1 Register

Offset : 7Ah

Reset Value : —



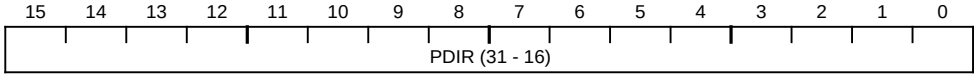
Bit 15- 0: PDATA31-PDATA16, PIO Data Bits.

These bits PDATA31- PDATA16 are mapped to PIO31 – PIO16 which indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

PIO Direction 1 Register

Offset : 78h

Reset Value : FFFFh

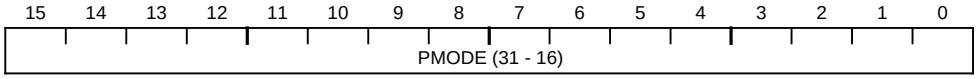


Bit 15-0: PDIR 31- PDIR16, PIO Direction Register.

Set 1: Configure the PIO pin as an input.

Set 0: Configure the PIO pin as an output or as normal pin function.

PIO Mode 1 Register **Offset : 76h**
Reset Value : 0000h



Bit 15-0: PMODE31-PMODE16, PIO Mode Bit.

The definitions of the PIO pins are configured by the combination of PIO Mode and PIO Direction. The PIO pins are programmed individually.

The definitions (PIO Mode, PIO Direction) for the PIO pin function:

(0 , 0) – Normal operation , (0 , 1) – PIO input with pull-up/pull-down

(1 , 0) – PIO output , (1 , 1) -- PIO input without pull-up/pull-down

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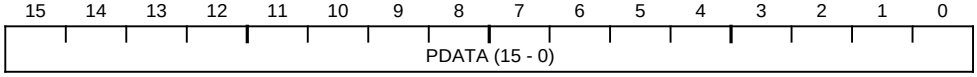
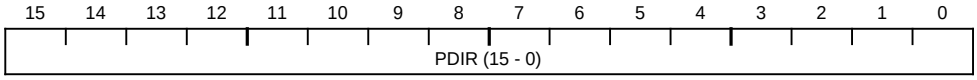
PIO Data 0 Register **Offset : 74h**
Reset Value : —



Bit 15-0: PDATA15- PDATA0: PIO Data Bus.

These bits PDATA15- PDATA0 are mapped to PIO15 – PIO0 which indicate the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

PIO Direction 0 Register **Offset : 72h**
Reset Value : FC0Fh



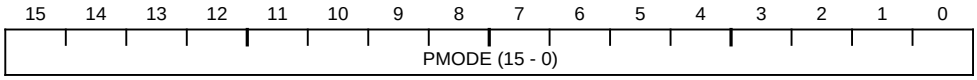
Bit 15-0: PDIR 15- PDIR0, PIO Direction Register.

Set 1: Configure the PIO pin as an input.

Set 0: Configure the PIO pin as an output or as normal pin function.

PIO Mode 0 Register

Offset : 70h
Reset Value : 0000h



Bit 15-0: PMODE15-PMODE0, PIO Mode Bit.

20. DRAM Controller

The R8822 supports 16-bit EDO or FP DRAM control interface. The supporting types are 256k*16,128k*16, 64k*16 or 32k*16. The DRAM control pins are multiplexed pins, which have been described in the Pin Configuration. The Basic System Application Block Diagram shows the connection between the microcontroller and DRAM. The DRAM controller supports two banks and dual $\overline{\textbf{CAS}}$ signals (supports high byte signal $\overline{\text{UCAS}}$ and low byte signal $\overline{\text{LCAS}}$ operating mode) access. When bit 6 of LMCS (A2h) register is set to 1, bank 0 will be enabled, then all the bit definitions of A2h are for bank 0 of the DRAM controller. Bit 6 of UMCS (A0h) is set to 1, then bank 1 is enabled and all bit definitions of A0h are for bank 1 of DRAM controller.

The memory space of bank 0 is from 00000h to 7FFFFh and the DRAM memory block size is programmable. Users can program register A2h (LMCS) to select memory block size 64k, 128k, 256k or 512k bytes. The memory space of bank 1 is from 80000h to FFFFFh. Users can configure register A0h (UMCS) to select the memory block size to be 64k, 128k, 256k or 512k bytes.

The address mapping of MA8 – MA0 & Row, Column signals:

DRAM Address	Row Address Mapping	Column Address Mapping
MA0(A1)	A1	A2
MA1(A3)	A3	A4
MA2(A5)	A5	A6
MA3(A7)	A7	A8
MA4(A9)	A9	A10
MA5(A11)	A11	A12
MA6(A13)	A13	A14
MA7(A15)	A15	A16
MA8(A17)	A17	A18

BANK 0	$\overline{\text{RAS0}}$ (Pin 58)	$\overline{\text{UCAS}}$ (Pin 51)	$\overline{\text{LCAS}}$ (Pin 68)	$\overline{\text{WE}}$ (Pin 5)	$\overline{\text{OE}}$ (Pin 6)
BANK 1	$\overline{\text{RAS1}}$ (Pin 69)	$\overline{\text{UCAS}}$ (Pin 51)	$\overline{\text{LCAS}}$ (Pin 68)	$\overline{\text{WE}}$ (Pin 5)	$\overline{\text{OE}}$ (Pin 6)

*** The pin numbers are for PQFP configuration ***

20.1 Programmable Read/ Write Cycle Time

The DRAM Controller read/write cycle depends on the external wait-state signal (ARDY or SRDY) and bit 0 and bit 1 of registers A0h and A2h. The default wait-state of bank 1 is 3 wait-states. It should program the wait-state bits for bank 0 after the CPU is reset.

20.2 Programmable Refresh Control

The DRAM controller provides Self-refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh control. The hardware will auto-stop the self-refresh operation when the controller accesses the DRAM data during the DRAM in self-refresh mode. During a refresh cycle, the AD bus will drive the address to FFFFFh and the $\overline{UCS}$ signal will not assert. The CPU will enter idle-state during a refresh cycle and the idle clock cycle is 7 clocks,. If two banks of DRAM are being used in a system, both banks will be refreshed at the same time.

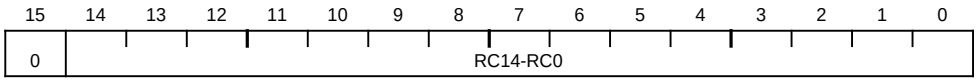
The reload counter (E2h) should be set more than 12h. Users should base on the system clock to configure the reload value, the normal refresh rate on a DRAM is 15.6us. It will start the refresh counter when the EN bit (bit 15 of E4h) is enabled.

Referenced wait-states & refresh counter value.

System clock	DRAM Speed	Wait-States	Refresh Cycle clocks	Refresh Reload Counter Value
25 MHz	70ns	0	7	186h
33MHz	70ns	1	7	203h
	60ns	0	7	203h
40MHz	70ns	2	7	270h
	60ns	1	7	270h
	50ns	0	7	270h
	40ns	0	7	270h

Refresh Reload Value Counter Register

Offset : E2h
Reset Value : —

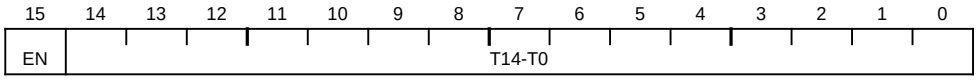


Bit 15: Reserved

Bit 14-0: RC14-RC0, Refresh Counter Reload Value. The counter value should be set more than 12h.

Refresh Counter Register

Offset : E4h
Reset Value : —



Bit 15: **EN**, Set 1 to enable refresh counter unit. This bit will be cleared to 0 after hardware reset.

Bit 14-0: T14-T0, Refresh Count. Read only bits and these bits present value of the down counter which triggers refresh requests.

21. Instruction Set OPCodes and Clock Cycles

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	

Function	Format				Clocks	Notes
immediate to accumulator	0000010w	data	data if w=1		1	
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)	1111011w	mod 100 r/m				
register-byte					13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m				
register-byte					16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)	1111011W	mod 110 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)	1111011w	mod 111 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
AAS = ASCII adjust for subtraction	00111111				3	
DAS = Decimal adjust for subtraction	00101111				2	
AAA = ASCII adjust for addition	00110111				3	
DAA = Decimal adjust for addition	00100111				2	
AAD = ASCII adjust for divide	11010101	00001010			14	
AAM = ASCII adjust for multiply	11010100	00001010			15	
CBW = Corrvert byte to word	10011000				2	
CWD = Convert word to double-word	10011001				2	

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	
JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp			1/9	
JNBE/JA = not below or equal/above	01110111	disp			1/9	
JNP/JPO = not parity/parity odd	01111011	disp			1/9	
JNO = not overflow	01110001	disp			1/9	

Function	Format			Clocks	Notes
JNS = not sign	01111001	disp		1/9	
Unconditional Transfers					
CALL = Call procedure					
direct within segment	11101000	disp-low	disp-high	11	
reg/memory indirect within segment	11111111	mod 010 r/m		12/17	
indirect intersegment	11111111	mod 011 r/m	(mod≠11)	25	
direct intersegment	10011010	segment offset		18	
		selector			
RET = **Retum from procedure**					
within segment	11000011			16	
within segment adding immed to SP	11000010	data-low	data-high	16	
intersegment	11001011			23	
instersegment adding immed to SP	1001010	data-low	data-high	23	
JMP = **Unconditional jump**					
short/long	11101011	disp-low		9/9	
direct within segment	11101001	disp-low	disp-high	9	
reg/memory indirect within segment	11111111	mod 100 r/m		11/16	
indirect intersegment	11111111	mod 101 r/m	(mod ?11)	18	
direct intersegment	11101010	segment offset		11	
		selector			
Iteration Control					
LOOP = Loop CX times	11100010	disp		7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp		7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp		7/16	
JCXZ = Jump if CX = zero	11100011	disp		7/15	
Interrupt					
INT = Interrupt					
Type specified	11001101	type		41	
Type 3	11001100			41	
INTO = Interrupt on overflow	11001110			43/4	
BOUND = Detect value out of range	01100010	mod reg r/m		21-60	
IRET = Interrupt return	11001111			31	
PROCESSOR CONTROL INSTRUCTIONS					
CLC = clear carry	11111000			2	
CMC = Complement carry	11110101			2	
STC = Set carry	11111001			2	
CLD = Clear direction	11111100			2	
STD = Set direction	11111101			2	
CLI = Clear interrupt	11111010			5	
STI = Set interrupt	11111011			5	
HLT = Halt	11110100			1	
WAIT = Wait	10011011			1	
LOCK = Bus lock prefix	11110000			1	
ESC = Math coprocessor escape	11011MMM	mod PPP r/m		1	
NOP = No operation	10010000			1	
SEGMENT OVERRIDE PREFIX					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

22. R8822 Execution Timings

The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with data or displacement required for execution, has been prefetched and resides in the instruction queue at the time needed.

2. No wait states or bus HOLDs occur.

3. All word -data are located on even-address boundaries.

4. One RISC micro operation (*u*OP) maps one cycle (according to the pipeline stages described below), except the following case:

Pipeline Stages for single micro operation (one cycle):

Fetch → Decode → op_r → ALU → WB (For ALU function *u*OP)

Fetch → Decode → EA → Access → WB (For Memory function *u*OP)

4.1 *Memory read u*OP need 6 cycles for bus.

Pipeline stages for *Memory read u*OP(6 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB

Bus Cycle

4.2 *Memory push u*OP need 1 cycle if it has no previous *Memory push u*OP, and 5 cycles if it has previous *Memory push* or *Memory Write u*OP.

Pipeline stages for *Memory push u*OP after *Memory push u*OP (another 5 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB (1st *Memory push u*OP)

(2nd *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

pipeline stall

4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8 bits operation need both 8 cycles, for 16 bits operation need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*Unconditional Fetch u*OP) will need 9 cycles.

Pipeline stages for unconditional fetch:

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → Fetch (*Fetch u*OP)

(next *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

will be flushed

These 9 cycles caused branch penalty

→ Fetch → Decode → following stages...(New *u*OP)

Note: op_r: operand read stage, EA: Calculate Effective Address stage, Idle: Bus Idle stage, T0..T3: Bus T0..T3 stage, Access: Access data from cache memory stage.

23. DC Characteristics

23.1 Absolute Maximum Rating

Symbol	Rating	Commercial	Unit	Note
V_{Term}	Terminal Voltage with Respect to GND	-0.5~V_{CC}+0.5	V	
T_A	Ambient Temperature	0~+70	°C	

23.2 Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5	5.25	V
GND	Ground	0	0	0	V
Vih	Input High Voltage (***Note 1***)	2.0	---	Vcc+0.5	V
Vih1	Input High Voltage ($\overline{RST}$)	3	---	Vcc+0.5	V
Vih2	Input High Voltage (X1)	3	---	Vcc+0.5	V
Vil	Input Low voltage	-0.5	0	0.8	V

Note 1: The $\overline{RST}$ ***and X1 pins are not included.***

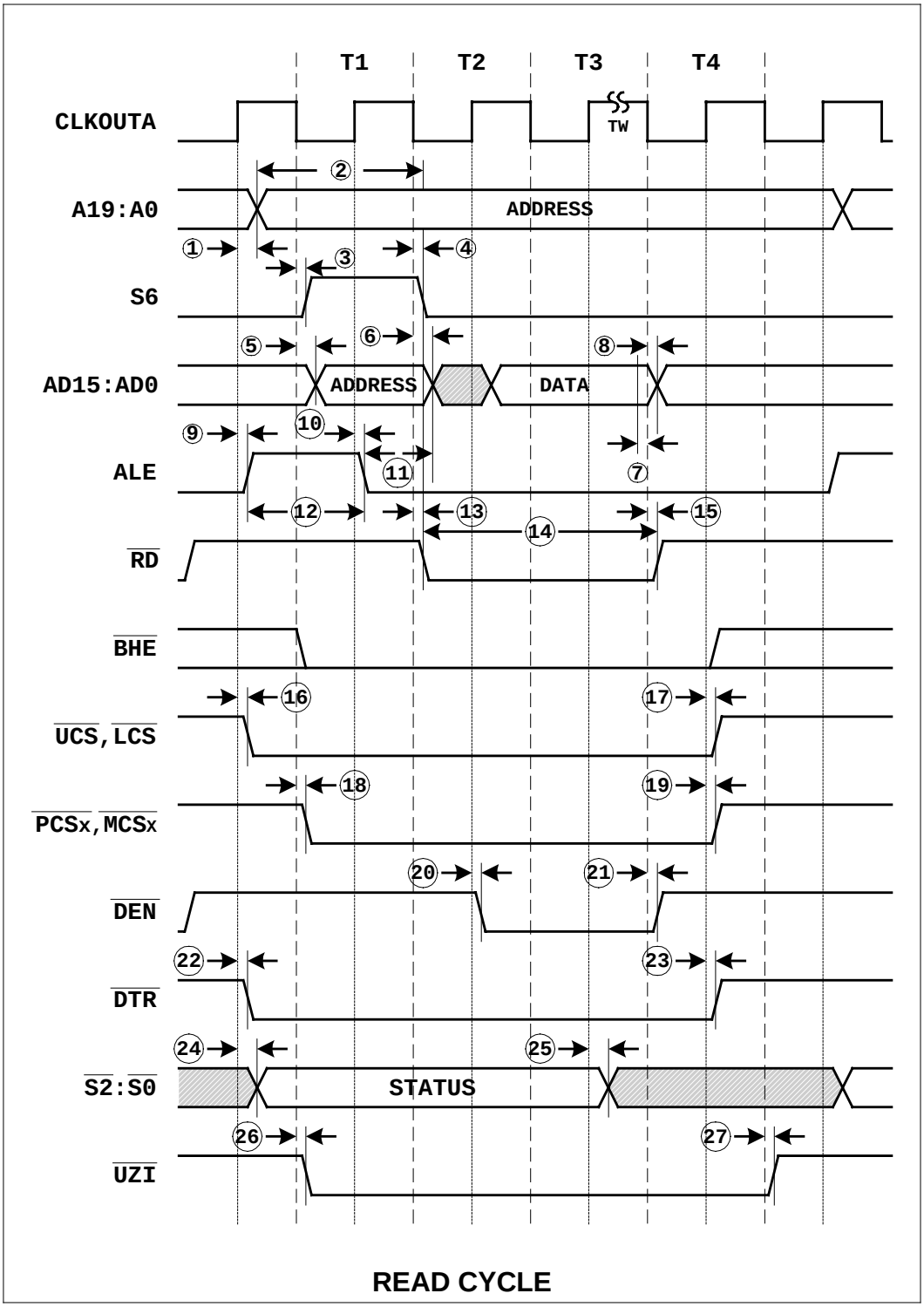
23.3 DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Ili	Input Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
Ili (with 10K pull R)	Input Leakage Current With Pull_R 10K enable	Vcc=Vmax Vin=GND to Vmax	-400	400	uA
Ili (with 50K pull R)	Input Leakage Current With Pull_R 50K	Vcc=Vmax Vin=GND to Vmax	-120	120	uA
Ilo	Output Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
VOL	Output Low Voltage	Iol=6mA, Vcc=Vmin.	---	0.4	V
VOH	Output High Voltage	Ioh=-6mA, Vcc=Vmin.	2.4	---	V
Icc	Max Operating Current	Vcc=5.25V 40MHz	---	180	mA

Note 2: Vmax=5.25V Vmin=4.75V

Symbol	Parameter	Min.	Max.	Unit	Note
F_{Max}	Max operation clock frequency of commercial	---	40	Mhz	V_{CC} ± 5%

24. AC Characteristics



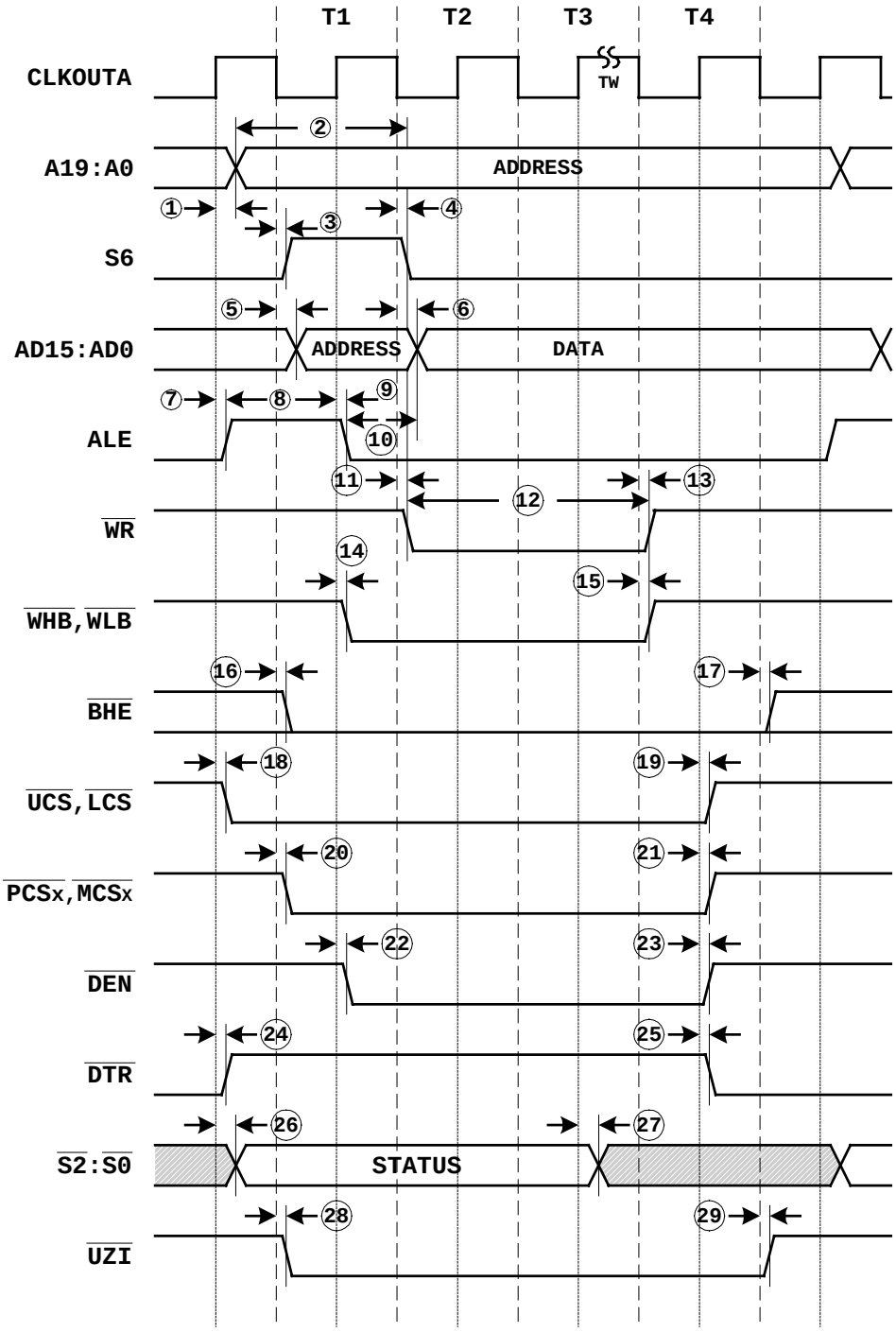
READ CYCLE

No.	Description	MIN	MAX	Unit
1	CLKOUTA high to A Address Valid	0	12	ns
2	A address valid to $\overline{RD}$ low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address Valid Delay	0	12	ns
6	Address Hold	0	12	ns
7	Data in setup	5		ns
8	Data in Hold	2		ns
9	ALE active delay	0	12	ns
10	ALE inactive delay	0	12	ns
11	Address Valid after ALE inactive	T/2-5		ns
12	ALE width	T-5		ns
13	$\overline{RD}$ active delay	0	12	ns
14	$\overline{RD}$ Pulse Width	2T-10		ns
15	$\overline{RD}$ inactive delay	0	12	ns
16	CLKOUTA HIGH to $\overline{LCS}$ / $\overline{UCS}$ valid	0	15	ns
17	UCS and LCS inactive delay	0	15	ns
18	$\overline{PCS}$ / $\overline{MCS}$ active delay	0	15	ns
19	$\overline{PCS}$ / $\overline{MCS}$ inactive delay	0	15	ns
20	$\overline{DEN}$ active delay	0	15	ns
21	$\overline{DEN}$ inactive delay	0	15	ns
22	DTR active delay	0	15	ns
23	DTR inactive delay	0	15	ns
24	Status active delay	0	15	ns
25	Status inactive delay	0	15	ns
26	$\overline{UZI}$ active delay	0	15	ns
27	$\overline{UZI}$ inactive delay	0	15	ns

1. T means a clock period time

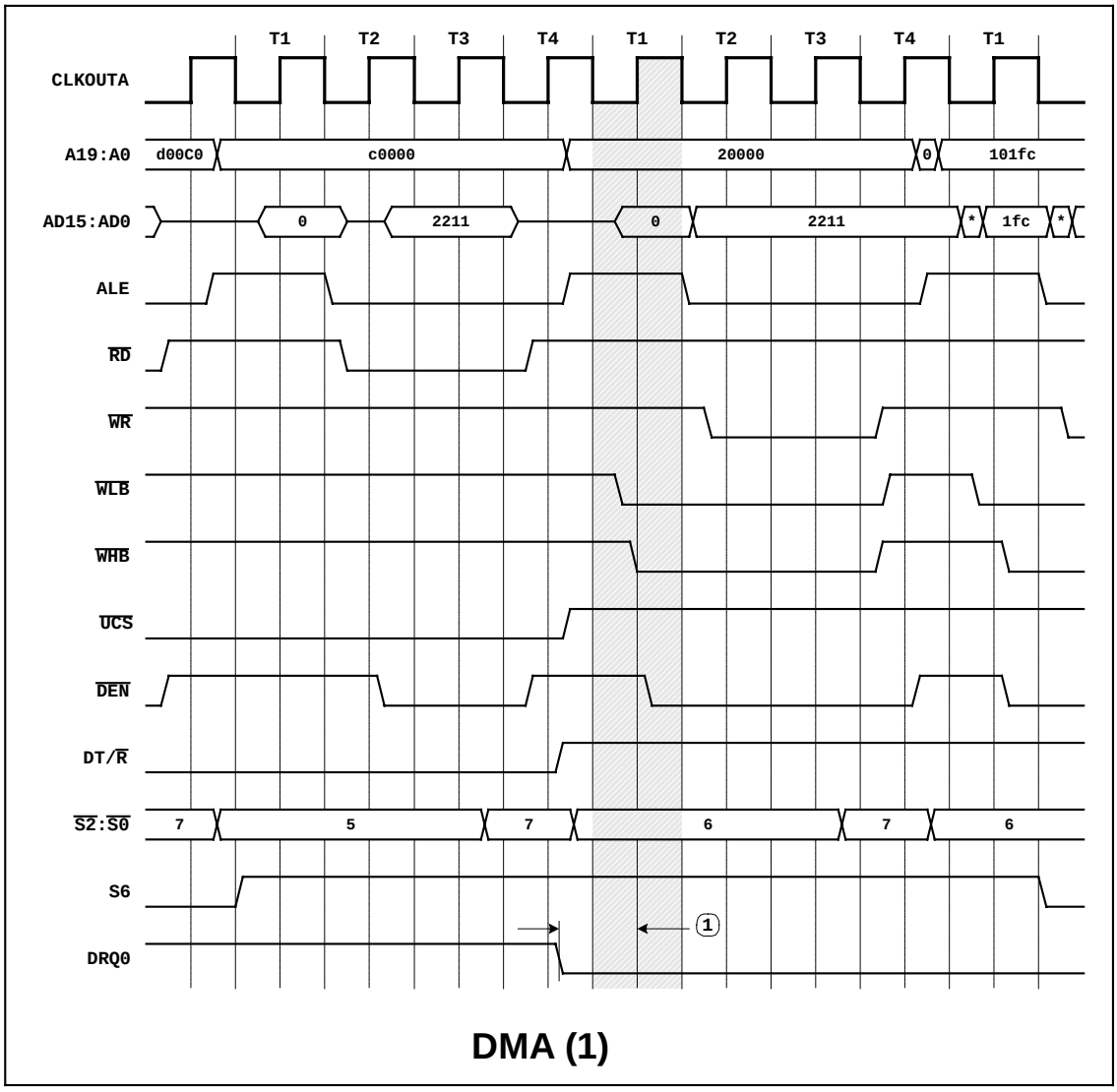
2. All timing parameters are measured at 1.5V with 50 PF loading on CLKOUTA

. All output test conditions are with CL=50 pF


T1
T2
T3
T4
TW
CLKOUTA
A19:A0
ADDRESS
S6
AD15:AD0
ADDRESS
DATA
ALE
WR
WHB, WLB
BHE
UCS, LCS
PCSx, MCSx
DEN
DTR
S2:S0
STATUS
UZI
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29

WRITE CYCLE

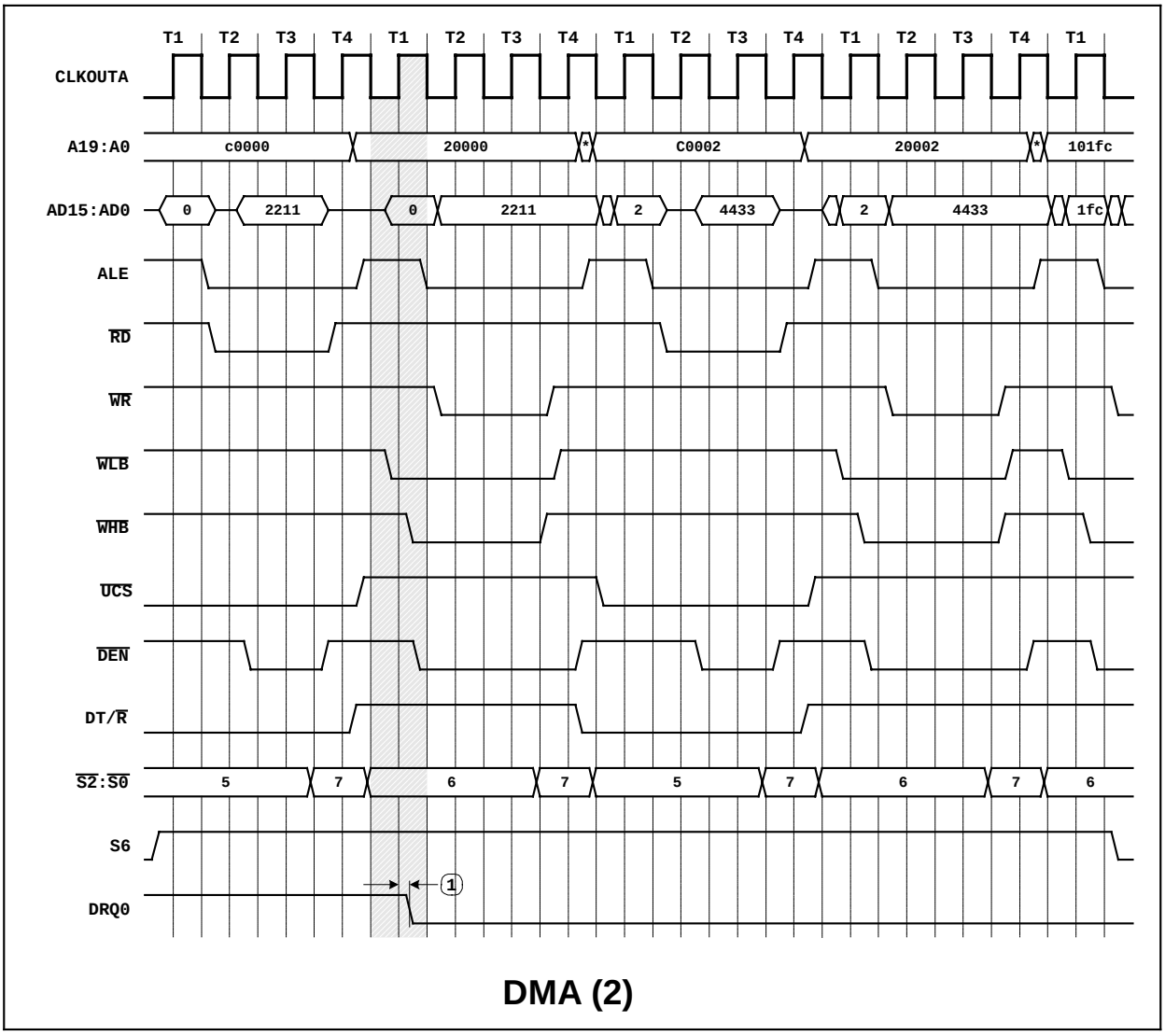
No.	Description	MIN	MAX	Unit
1	CLKOUTA high to A Address Valid	0	12	ns
2	A address valid to $\overline{WR}$ low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address Valid Delay	0	12	ns
6	Address Hold			ns
7	ALE active delay	0	12	ns
8	ALE width	T-10		ns
9	ALE inactive delay	0	12	ns
10	Address valid after ALE inactive	1/2T-5		ns
11	$\overline{WR}$ active delay	0	12	ns
12	$\overline{WR}$ pulse width	2T-10		ns
13	$\overline{WR}$ inactive delay	0	12	ns
14	$\overline{WHB}$ / $\overline{WLB}$ active delay	0	15	ns
15	$\overline{WHB}$ / $\overline{WLB}$ inactive delay	0	15	ns
16	BHE active delay	0	15	ns
17	BHE inactive delay	0	15	ns
18	CLKOUTA high to $\overline{UCS}$ / $\overline{LCS}$ valid	0	15	ns
19	$\overline{UCS}$ / $\overline{LCS}$ inactive delay	0	15	ns
20	$\overline{PCS}$ / $\overline{MCS}$ active delay	0	15	ns
21	$\overline{PCS}$ / $\overline{MCS}$ inactive delay	0	15	ns
22	$\overline{DEN}$ active delay	0	15	ns
23	$\overline{DEN}$ inactive delay	0	15	ns
24	$\overline{DTR}$ active delay	0	15	ns
25	$\overline{DTR}$ inactive delay	0	15	ns
26	Status active delay	0	15	ns
27	Status inactive delay	0	15	ns
28	$\overline{UZI}$ active delay	0	15	ns
29	$\overline{UZI}$ inactive delay	0	15	ns



DMA (1)

*** The source-synchronized transfer is not followed immediately by another DMA transfer**

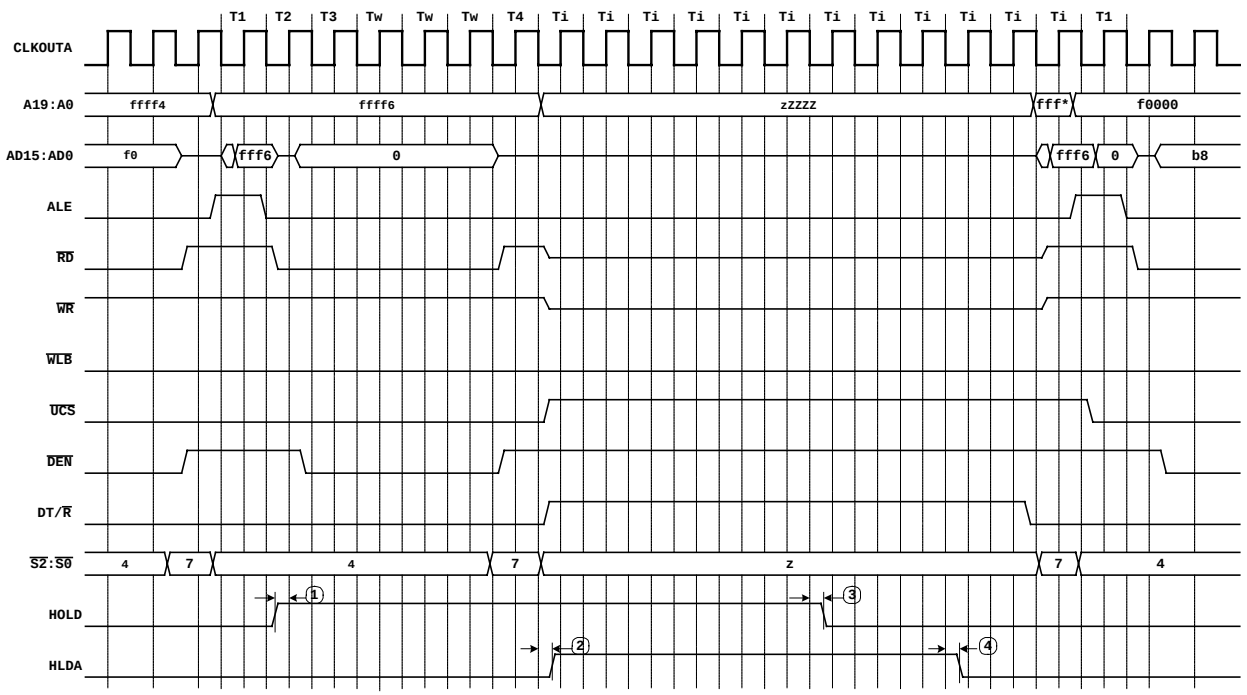
No.	Description	MIN	MAX	Unit
1	DRQ is confirmed time	5		ns



DMA (2)

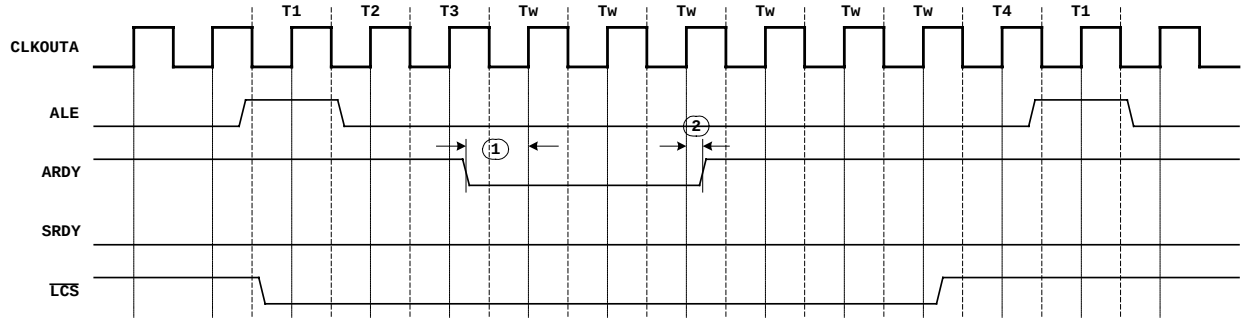
*** The source-synchronized transfer is followed immediately by another DMA transfer**

No.	Description	MIN	MAX	Unit
1	DRQ is confirmed time	2	0	ns



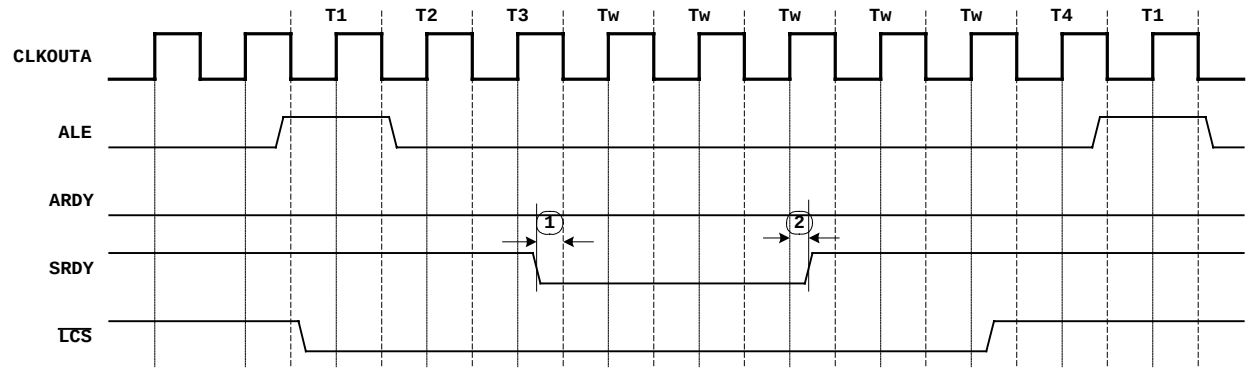
HOLD/HLDA Timing

No.	Description	MIN	MAX	Unit
1	HOLD setup time	5	0	ns
2	HLDA Valid Delay	0	15	ns
3	HOLD hold time	2	0	ns
4	HLDA Valid Delay	0	15	ns



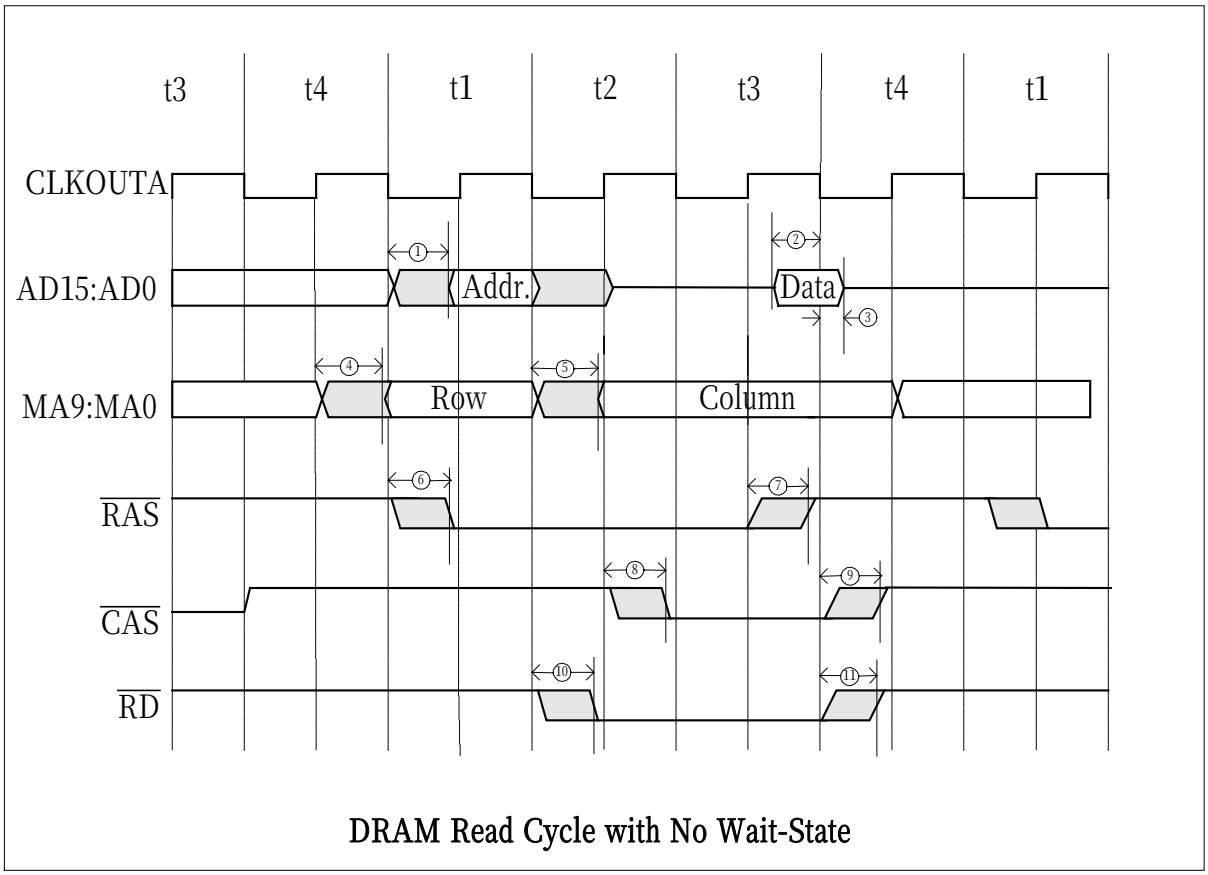
ARDY Timing

No.	Description	MIN	MAX	Unit
1	ARDY Resolution Transition setup time	5	0	ns
2	ARDY active hold time	5	0	ns



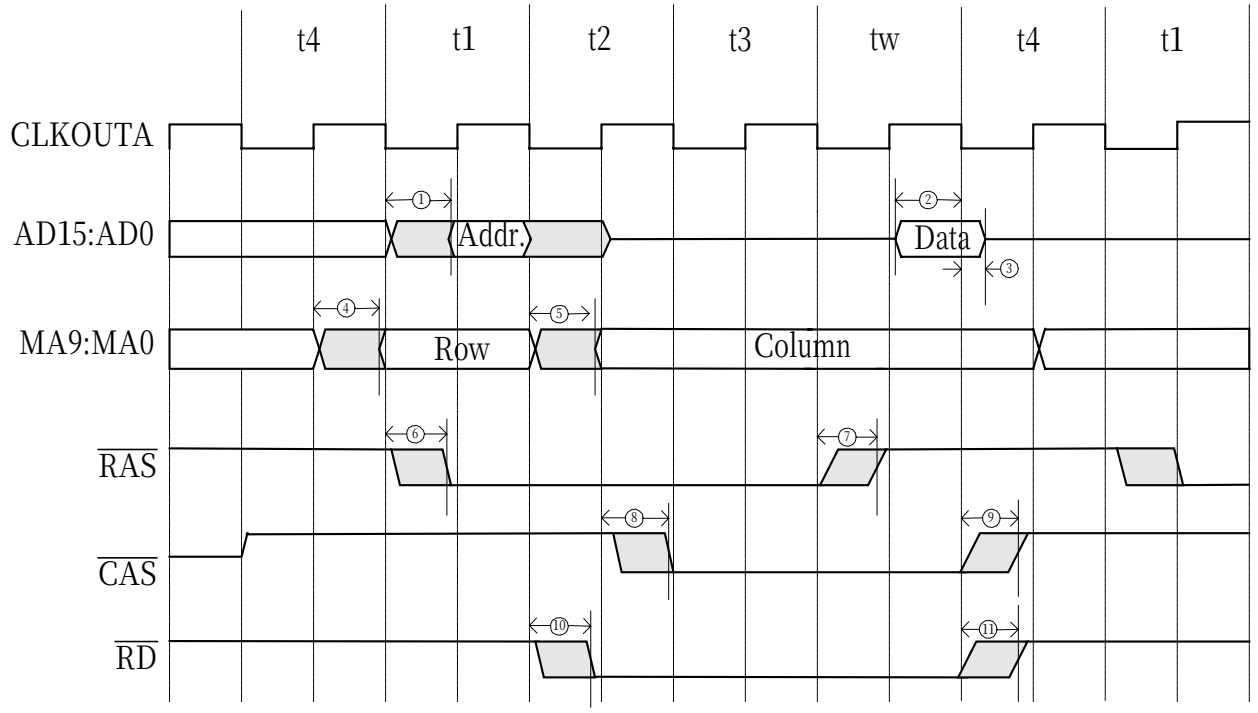
SRDY Timing

No.	Description	MIN	MAX	Unit
1	SRDY transition setup time	5	0	ns
2	SRDY transition hold time	5	0	ns



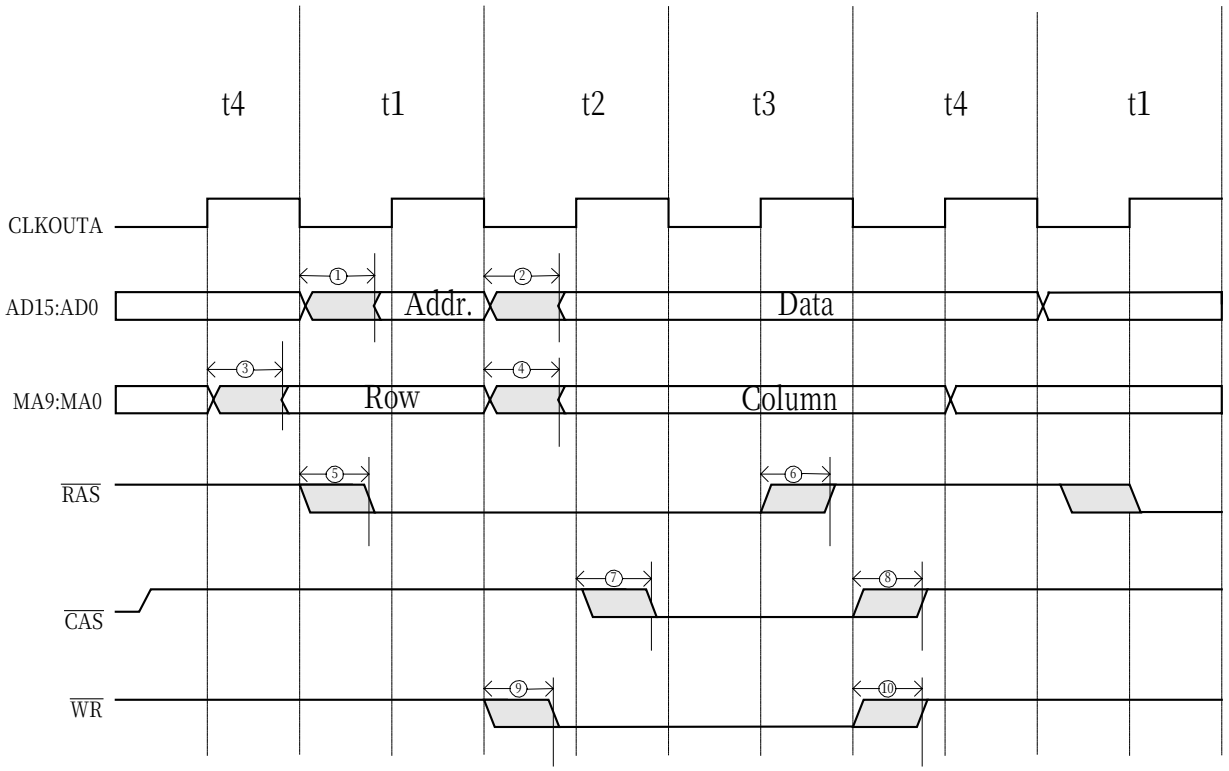
DRAM Read Cycle with No Wait-State

No.	Description	MIN	MAX	Unit
1	CLKOUTA low to A Address Valid	0	12	ns
2	Data setup time	5		ns
3	Data hold time	2		ns
4	CLKOUTA high to Row address valid	0	12	ns
5	CLKOUTA low to Column address valid	0	12	ns
6	CLKOUTA low to $\overline{RAS}$ active	3	12	ns
7	CLKOUTA high to $\overline{RAS}$ inactive	3	12	ns
8	CLKOUTA high to $\overline{CAS}$ active	3	12	ns
9	CLKOUTA low to $\overline{CAS}$ inactive	3	12	ns
10	CLKOUTA low to $\overline{RD}$ active	0	12	ns
11	CLKOUTA low to $\overline{RD}$ inactive	0	12	ns



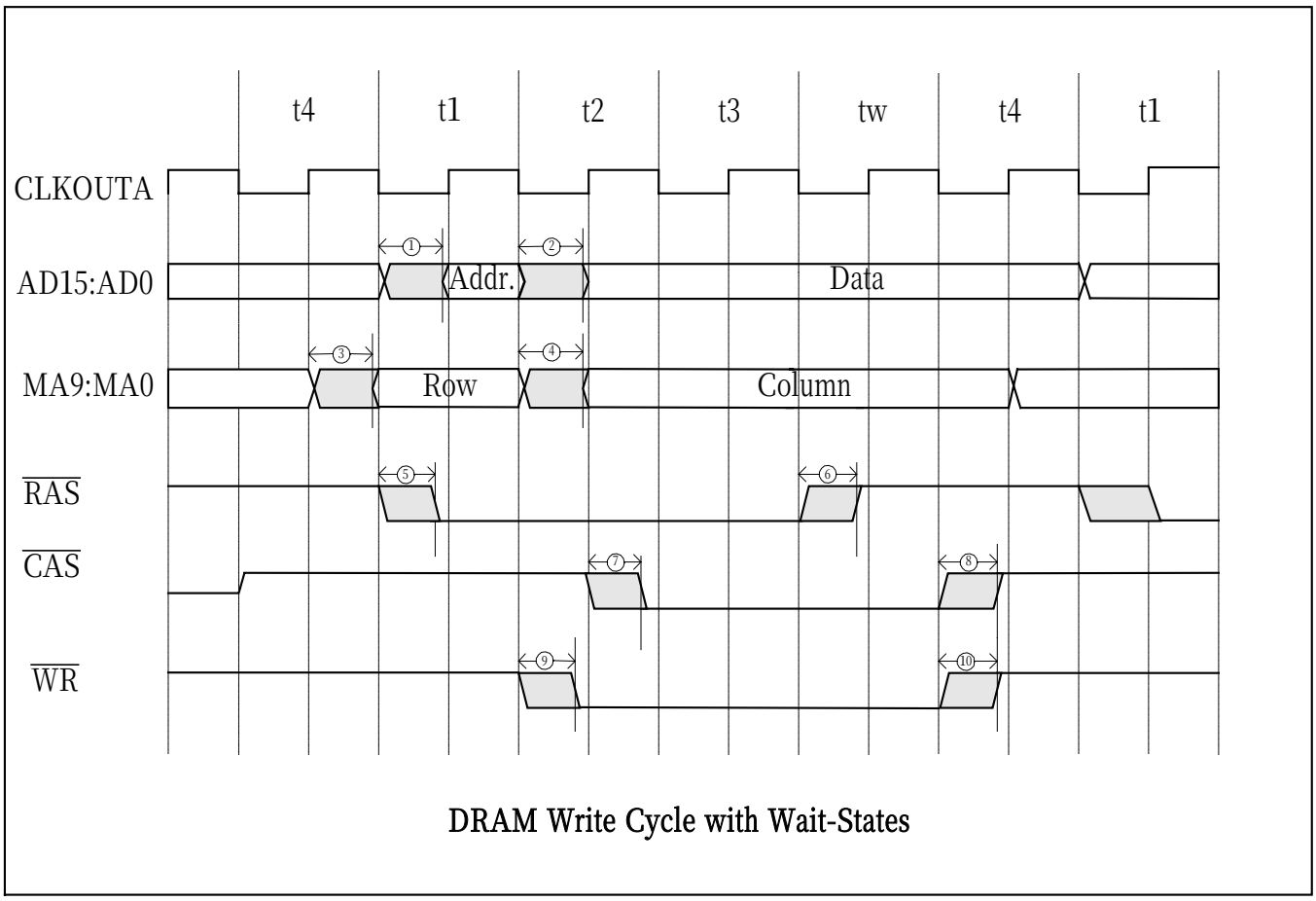
DRAM Read Cycle with Wait-States

No.	Description	MIN	MAX	Unit
1	CLKOUTA low to A Address Valid	0	12	ns
2	Data setup time	5		ns
3	Data hold time	2		ns
4	CLKOUTA high to Row address valid	0	12	ns
5	CLKOUTA low to Column address valid	0	12	ns
6	CLKOUTA low to $\overline{RAS}$ active	3	12	ns
7	CLKOUTA high to $\overline{RAS}$ inactive	3	12	ns
8	CLKOUTA high to $\overline{CAS}$ active	3	12	ns
9	CLKOUTA low to $\overline{CAS}$ inactive	3	12	ns
10	CLKOUTA low to $\overline{RD}$ active	0	12	ns
11	CLKOUTA low to $\overline{RD}$ inactive	0		ns



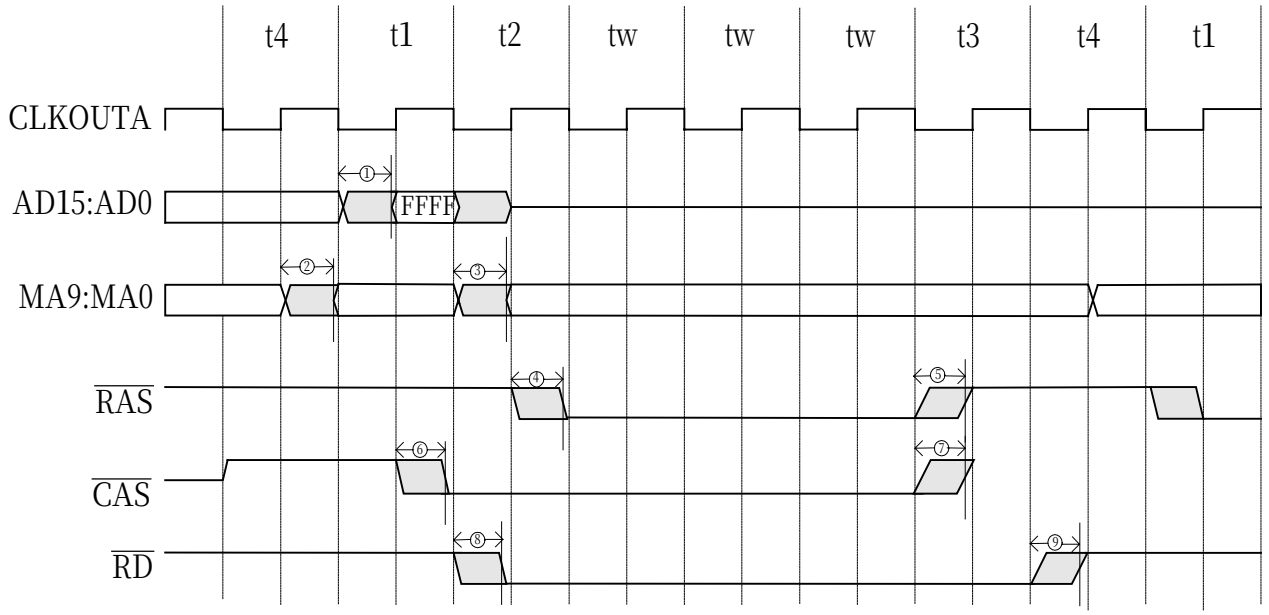
DRAM Write Cycle with No Wait-State

No.	Description	MIN	MAX	Unit
1	CLKOUTA low to A Address Valid	0	12	ns
2	CLKOUTA low to A Data Valid	0	12	ns
3	CLKOUTA high to Row address valid	0	12	ns
4	CLKOUTA low to Column address valid	0	12	ns
5	CLKOUTA low to $\overline{RAS}$ active	3	12	ns
6	CLKOUTA high to $\overline{RAS}$ inactive	3	12	ns
7	CLKOUTA high to $\overline{CAS}$ active	3	12	ns
8	CLKOUTA low to $\overline{CAS}$ inactive	3	12	ns
9	CLKOUTA low to $\overline{WR}$ active	0	12	ns
10	CLKOUTA low to $\overline{WR}$ inactive	0	12	ns



DRAM Write Cycle with Wait-States

No.	Description	MIN	MAX	Unit
1	CLKOUTA low to A Address Valid	0	12	ns
2	CLKOUTA low to A Data Valid	0	12	ns
3	CLKOUTA high to Row address valid	0	12	ns
4	CLKOUTA low to Column address valid	0	12	ns
5	CLKOUTA low to $\overline{RAS}$ active	3	12	ns
6	CLKOUTA high to $\overline{RAS}$ inactive	3	12	ns
7	CLKOUTA high to $\overline{CAS}$ active	3	12	ns
8	CLKOUTA low to $\overline{CAS}$ inactive	3	12	ns
9	CLKOUTA low to $\overline{WR}$ active	0	12	ns
10	CLKOUTA low to $\overline{WR}$ inactive	0	12	ns



DRAM Refresh Cycle

No.	Description	MIN	MAX	Unit
1	CLKOUTA high to Data drive FFFF	0	12	ns
2	CLKOUTA high to Row address valid	0	12	ns
3	CLKOUTA low to Column address valid	0	12	ns
4	CLKOUTA high to $\overline{RAS}$ active	3	12	ns
5	CLKOUTA low to $\overline{RAS}$ inactive	3	12	ns
6	CLKOUTA high to $\overline{CAS}$ active	3	12	ns
7	CLKOUTA low to $\overline{CAS}$ inactive	3	12	ns
8	CLKOUTA low to $\overline{RD}$ active	0	12	ns
9	CLKOUTA low to $\overline{RD}$ inactive	0	12	ns

25. Thermal Characteristics

θ_{JA}: thermal resistance from device junction to ambient temperature

P: operation power

T_A: maximum ambient temperature in operation mode

$T_A=T_J–(P×\theta_{JA})$

Package/Board	Air Flow (m/s)	θ_{JA}
PQFP/2-Layer	0	48.8
	1	44.9
	2	42.7
	3	41.9
LQFP/2-Layer	0	53.6
	1	48.9
	2	45.5
	3	44.5
PQFP/4-Layer	0	38.9
	1	35.7
	2	33.8
	3	33.3
LQFP/4-Layer	0	42.6
	1	38.0
	2	36.1
	3	35.3

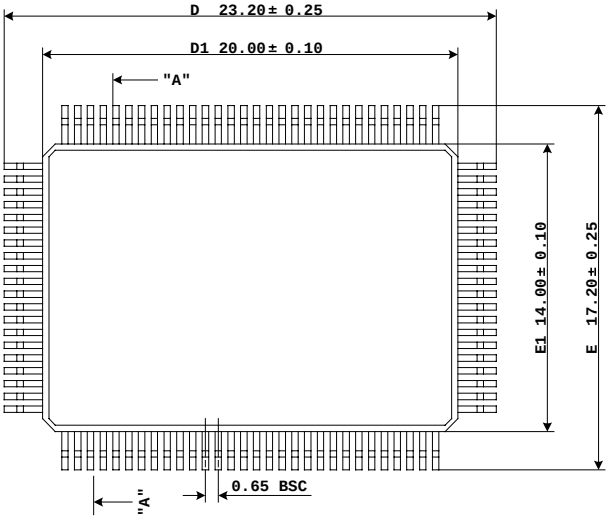
Unit: °C/Watt

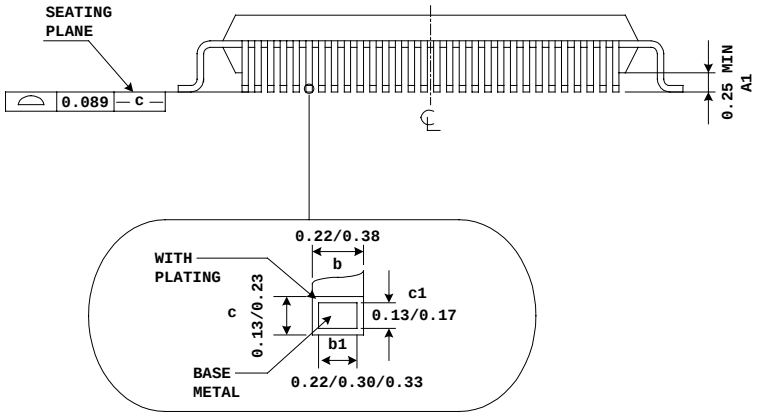
Recommended Storage Temperature: –65°C to +125°C

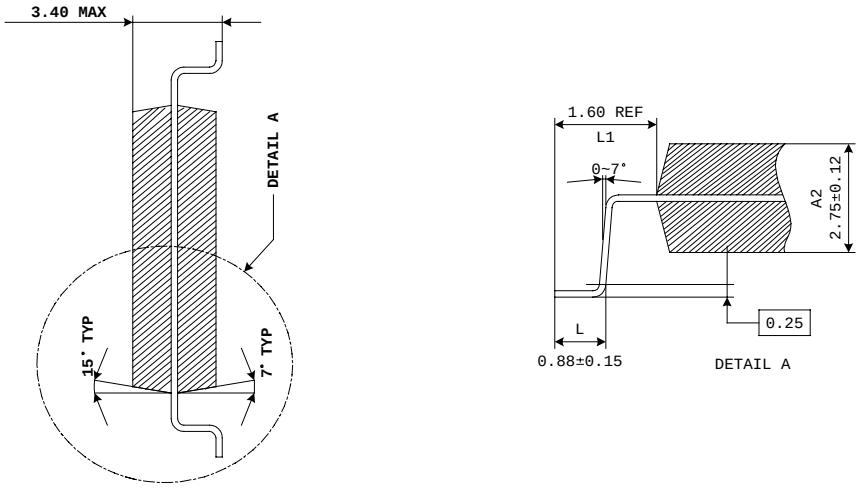
Note: The IC should be mounted on PCB within 7 days after the dry pack is opened. If the IC is out of dry pack more than 7 days, it should be burned in oven (+125°C, > 12 hours) before mounted on PCB.

26. Package Information

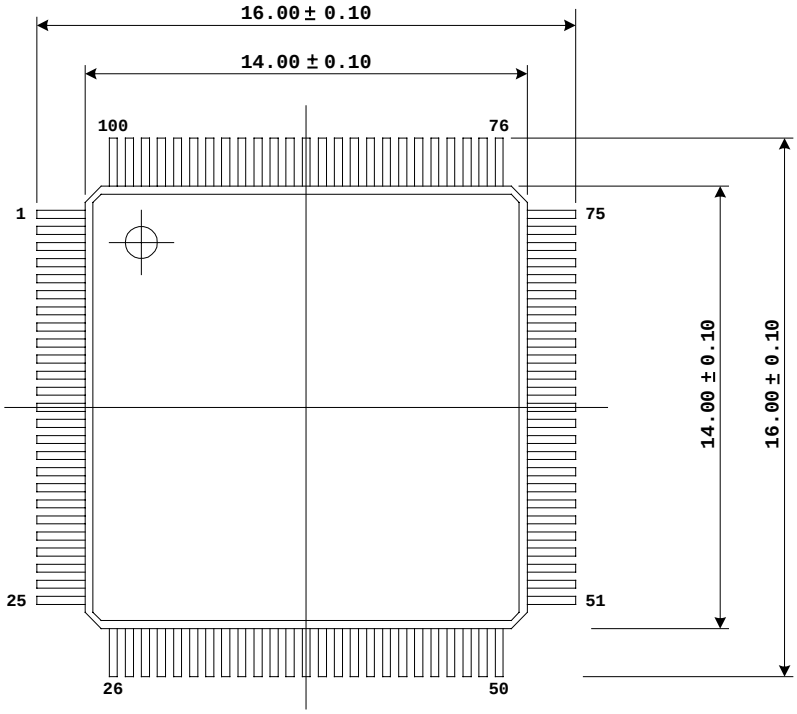
26.1 PQFP

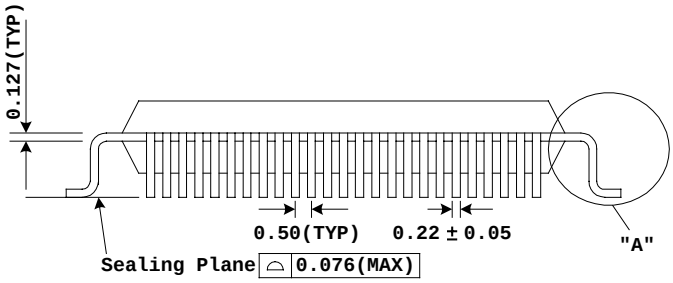


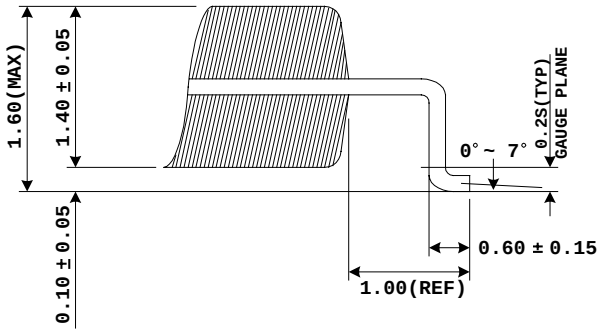




26.2 LQFP







UNIT:mm

27. Revision History

Rev.	Date	History
P10	2000/7/31	Preliminary Version
F11	2001/5/17	Final Version 1.1: Formal release
F12	2001/8/10	Modify Wait State Description (Page 30)
F13	2001/11/29	DC Characteristics
F14	2001/12/25	Modify Oscillator Characteristics
F15	2002/05/08	Modify Wait State Description
F16	2004/01/05	Modify DC Characteristics and add Thermal Characteristics.